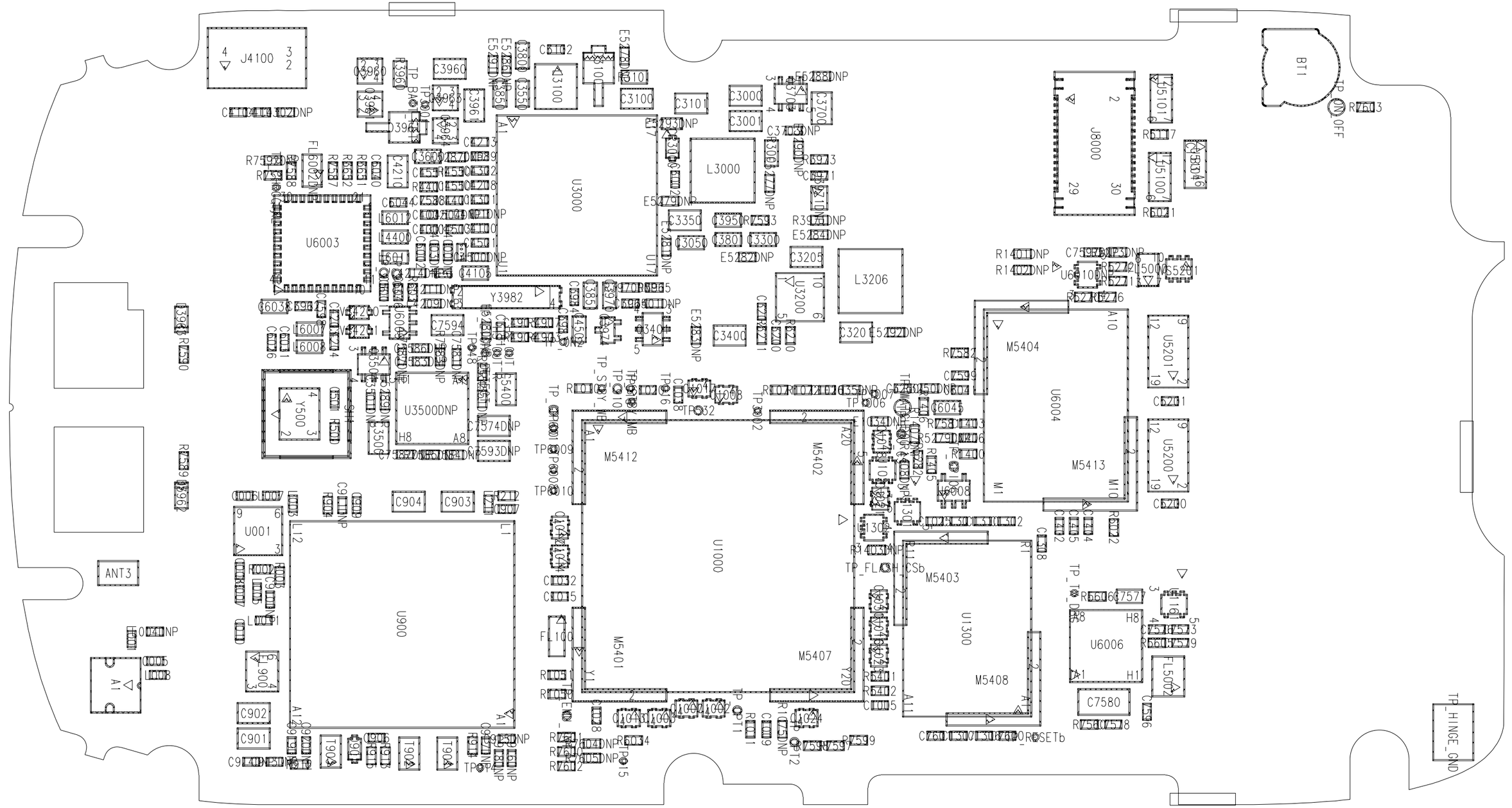
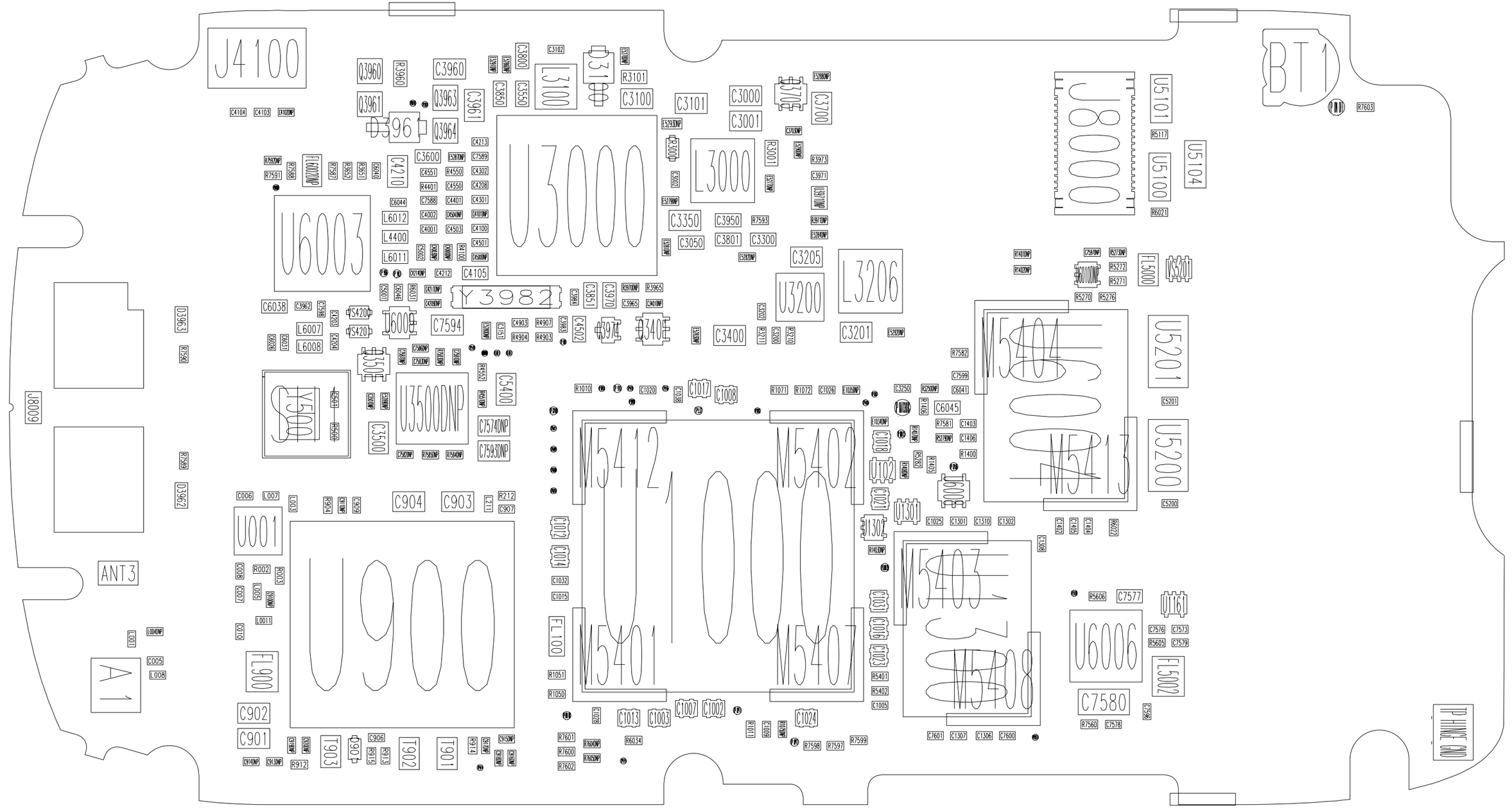
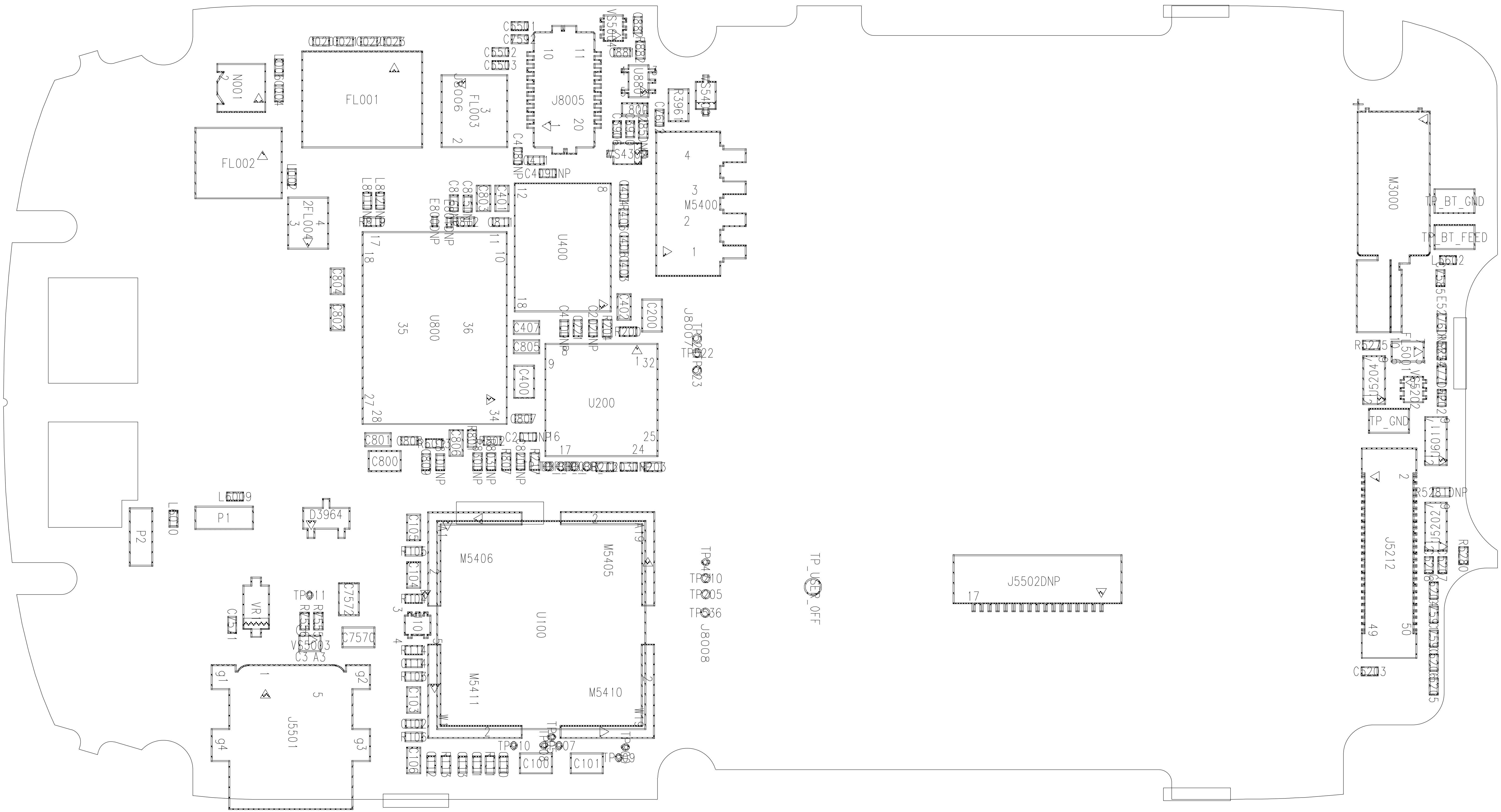
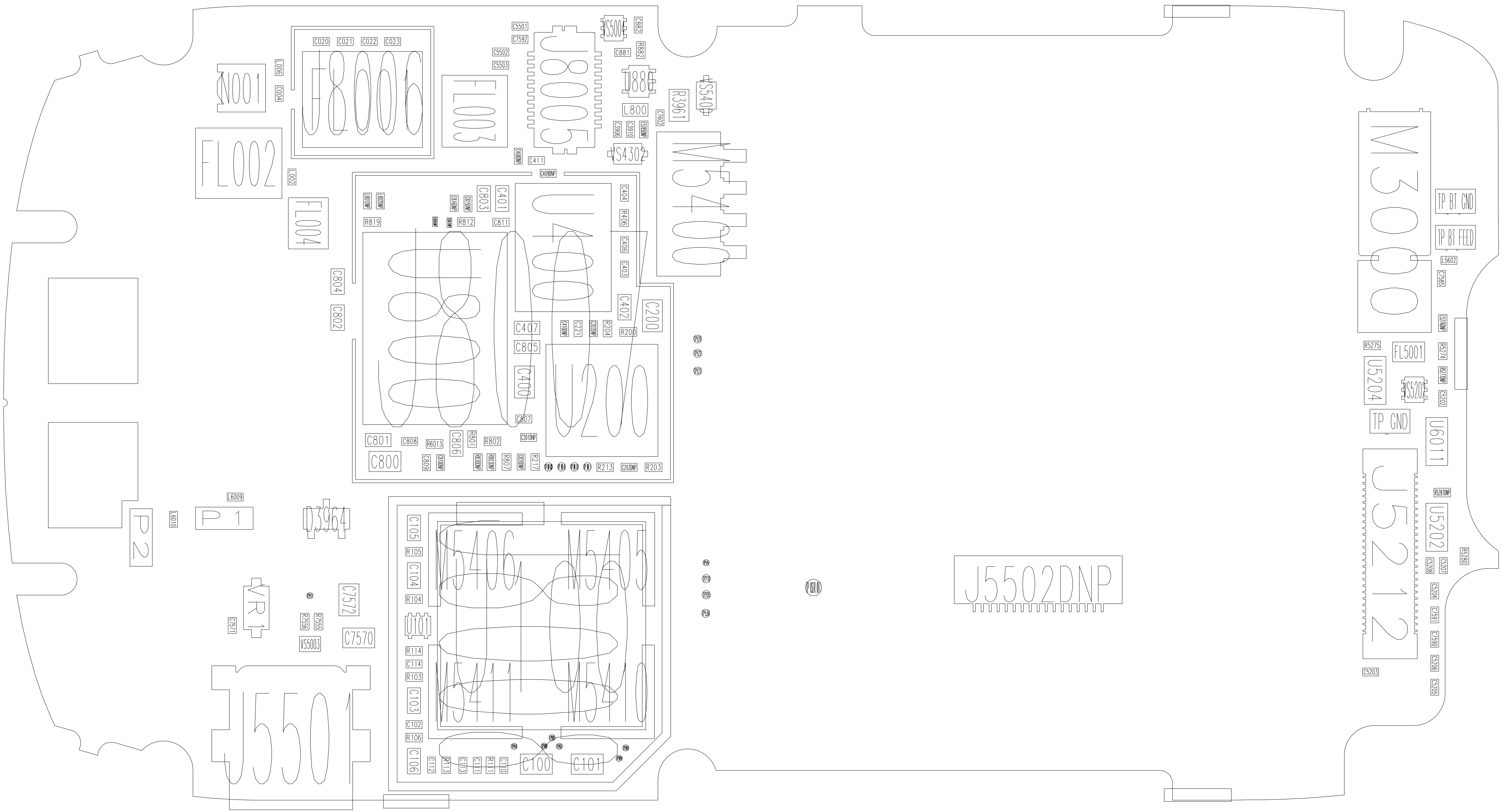

J4100
U3000
L3000
U6003
Y3982
U3500DNP
Y500
U3100
U3200
L3206
M5404
U6004
M5413
M5412
M5402
U1000
M5401
M5407
M5403
U1300
M5408
U6006
J8000
BT1
U001
U900
ANT3
C902
C901
C903
C904
TP_SLEEP_MB
TP_FLASH_CSb
TP_TOUCH_RESETb
TP_HINGE_GND


J4100
BT1
U8000
U5101
U5104
U5100
U6003
U3000
L3000
L3100
U3200
L3206
U5201
U5200
M5404
M5413
M5412
M5402
M5401
M5407
M5403
M5408
U6006
U900
U001
U3500DNP
Y5300
Y3982
FL100
FL900
FL5000
FL6002
ANT3
A1
TP_PHASE_GND



FL001
FL002
FL003
N001
J8005
J8006
M5400
U400
U800
U200
M3000
TP_BT_GND
TP_BT_FEED
TP_GND
J5212
J5502DNP
M5406
M5405
M5411
M5410
U100
J5501
P1
P2
D3964
VR1
C7572
C7570
C800
C801
C804
C802
C407
C805
C400
C401
C803
C200
C402
C100
C101
C106
R396
C5203
TP_USER_OFF
J8008


J8006
N001
FL002
FL003
FL004
J8005
M5400
U400
U200
U800
C800
C801
M5406
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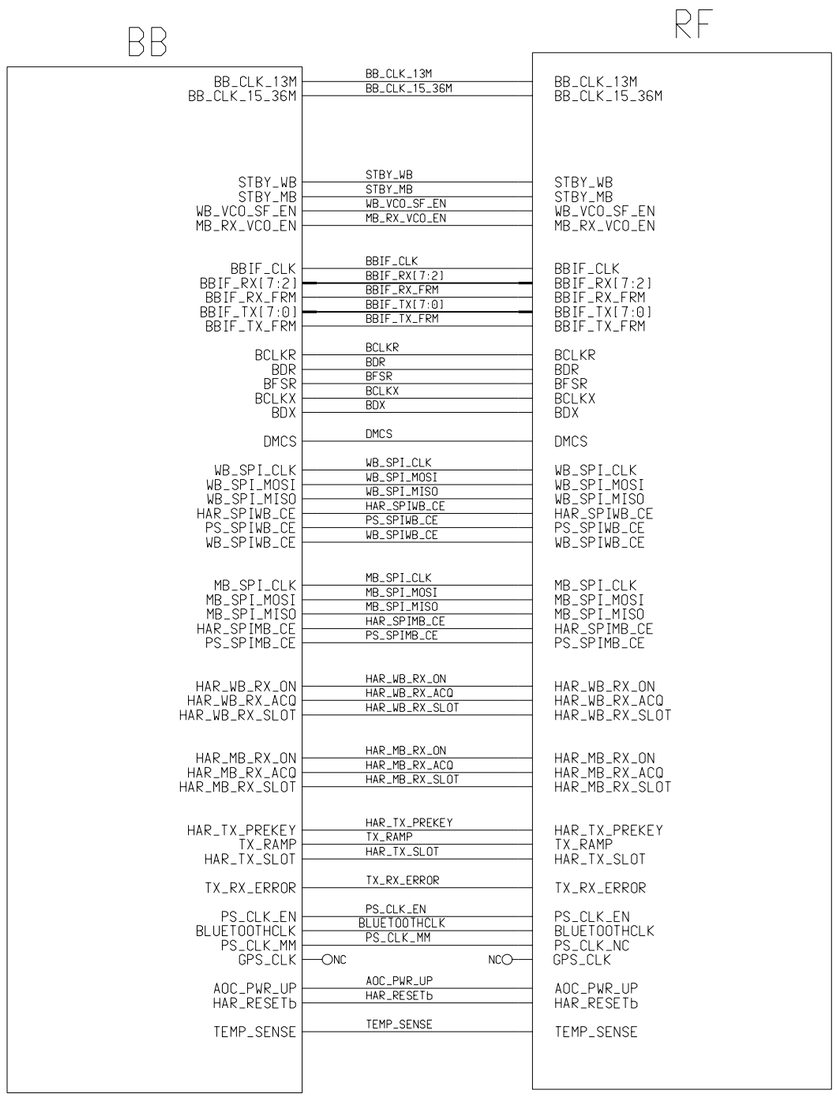
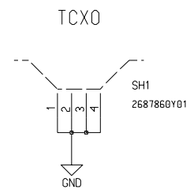
M5411
M5410
C100
C101
U101
J5501
VR1
P1
P2
D3964
C7572
C7570
M3000
J5212
J5502DNP
FL5001
U5204
U6011
U5202
TP BT GND
TP BT FEED
TP GND
L800
R3961
C200
C402
C400
C407
C805

Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS IA Top Level — Size:
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: P3 — Drawing Number: — Page: 1 — Of: 23
Changed by: frg025	Date: Wednesday, March 30, 2005 — Time: 6:16:00 pm





MOTOROLA CONFIDENTIAL PROPRIETARY

Engineer: Rafael Gomez	MOTOROLA INC.
Drawn by: Rafael Gomez	
R&D CHK:	TITLE: SIRIUS IA — Size:
DOC CTRL CHK:	BaseBand Top Level
MFG CTRL CHK:	REV: P3 | Drawing Number: 8487533Y02 | Page: 2 | Of: 23
QA CHK:	
Changed by: frg025	Date: Tuesday, April 5, 2005 — Time: 4:06:52 pm

Misc Connectors

Keypad Connector
LED Lighting
Triflash-R
USIM

MMC_CLK_NVIDIA, MMC_CMD_NVIDIA, MMC_DATA0_NVIDIA
ON_OFF_ENDb
LIGHT_DETECT

SIM_CLK, SIM_RST, SIM_IO
COL[3:0], ROW[7:0], FLIP_DETECT, LIGHT_SENSOR_EN

Display & Imager Interfaces

DATA[15:0], GPU_IND_ADDR, GPU_CSb, FLASH_DOC_GPU_OEb, GPU_RWb, FLASH_RWb_GPU_EBHb, DOC_GPU_EBLb, GPU_INTb, GPU_RESETb
PS_CLK_MM
EAR_SPKR-, EAR_SPKR+
MMC_DATA0_NVIDIA, MMC_CLK_NVIDIA, MMC_CMD_NVIDIA

CORE LOGIC BLOCK

POG
Memories

KPD_LED_EL_EN1, KPD_LED_EL_EN2, MMC_DETb
SIM_CLK, SIM_RST, SIM_IO
COL[3:0], ROW[7:0], FLIP_DETECT, LIGHT_SENSOR_EN
DATA[15:0], GPU_IND_ADDR, GPU_CSb, FLASH_DOC_GPU_OEb, GPU_RWb, FLASH_RWb_GPU_EBHb, DOC_GPU_EBLb, GPU_INTb, GPU_RESETB
MMC_DATA0_NVIDIA, MMC_CLK_NVIDIA, MMC_CMD_NVIDIA
HAR_RESETb, BCLKR, BFSR, BDR, BCLKX, BDX
TX_RX_ERROR
BBIF_RX_FRAME, BBIF_RX[7:2], BBIF_TX[7:0], BBIF_TX_FRAME, BBIF_CLK
BB_CLK_13M, MB_SPI_CLK, MB_SPI_MISO, MB_SPI_MOSI, HAR_SPIMB_CE, PS_SPIMB_CE, HAR_MB_RX_ACQ, HAR_MB_RX_SLOT, HAR_MB_RX_ON, MB_RX_VCO_EN
AOC_PWR_UP
BB_CLK_15_36M, WB_SPI_CLK, WB_SPI_MISO, WB_SPI_MOSI, HAR_SPIWB_CE, WB_SPIWB_CE, HAR_WB_RX_SLOT, HAR_TX_SLOT, HAR_WB_RX_ACQ, HAR_WB_RX_ON, TX_RAMP, DMCS, PS_SPIWB_CE, WB_VCO_SF_EN, HAR_TX_PREKEY
PS_CLK_EN

RXD_VMIN, USB_VPIN, USB_TXENb, EMU_CS, EMU_INT
TXD_VPOUT, PPD_EN, USB_VMOUT, RTSb_XRXD, BATT_IO
PS_CLK_ENb
GPS_CTSb, GPS_TX, GPS_RX, GPS_RTSb, GPS_RESETb
N_SHUT_DOWN, BLUE_HOST_WAKEb, BLUETOOTH_WAKEb, BLUE_TX, BLUE_RX, BLUE_CTSb, BLUE_RTSb
ASAP_FS, ASAP_CLK, ASAP_RX, ASAP_TX
STBY_MB, STBY_WB
STEREO_FS, STEREO_CLK, STEREO_TX_POG, VSIMC_EN, PCAP_CLK_IN
STEREO_RX_POG
BB_SPI_CLK, BB_SPI_MISO, BB_SPI_MOSI, PCAP_CS, BB_SPI2_CLK, BB_SPI2_MISO, BB_SPI2_MOSI, PCAP_CS2
PCAP_INT, PCAP_RESETb, USER_OFF, POWER_FAIL, WATCHDOG, CLK_32_768K
YAMAHA_CLK_IN, YAMAHA_CSb, BATT_DETb, YAMAHA_INTb

EMU Bus and Battery Charger

RXD_VMIN, USB_VPIN, PCAP_RESETb, USB_TXENB, EMU_CS, EMU_INT, BB_SPI_MISO, BB_SPI_MOSI, BB_SPI_CLK, TXD_VPOUT, PPD_EN, USB_VMOUT, RTSb_XRXD, BATT_IO
HS_SPKR_R, HS_SPKR_L, THERM_BIAS, EMU_PWR_ON, AD4, AD6, BATT_I, BATT_P, AUDIO_IN, BL_SINK

Bluetooth

N_SHUT_DOWN, BLUE_HOST_WAKEb, BLUETOOTH_WAKEb, BLUE_TX, BLUE_RX, BLUE_CTSb, BLUE_RTSb, ASAP_FS, ASAP_CLK, ASAP_RX, ASAP_TX
BLUE_SCAN_SYNC, CLK_32_768K_BUFF, BLUETOOTHCLK, BLUE_CLK_EN

PCAP2 (Power/Audio)

ASAP_FS, ASAP_CLK, ASAP_RX, ASAP_TX, STEREO_FS, STEREO_CLK, STEREO_TX_POG, VSIMC_EN, PCAP_CLK_IN, STEREO_RX_POG, BB_SPI_CLK, BB_SPI_MISO, BB_SPI_MOSI, PCAP_CS, BB_SPI2_CLK, BB_SPI2_MISO, BB_SPI2_MOSI, PCAP_CS2, PCAP_INT, PCAP_RESETb, USER_OFF, POWER_FAIL, WATCHDOG, CLK_32_768K, YAMAHA_CLK_IN, YAMAHA_CSb, BATT_DETb, YAMAHA_INTb, HAR_TX_PREKEY
CLK_32_768K_BUFF, EMU_PWR_ON, AUDIO_IN, THERM_BIAS, BATT_P, BATT_I, AD4, AD6, TEMP_SENSE, BL_SINK, ON_OFF_ENDb, PS_CLK_MM, HS_SPKR_R, HS_SPKR_L, EAR_SPKR-, EAR_SPKR+, LIGHT_DETECT

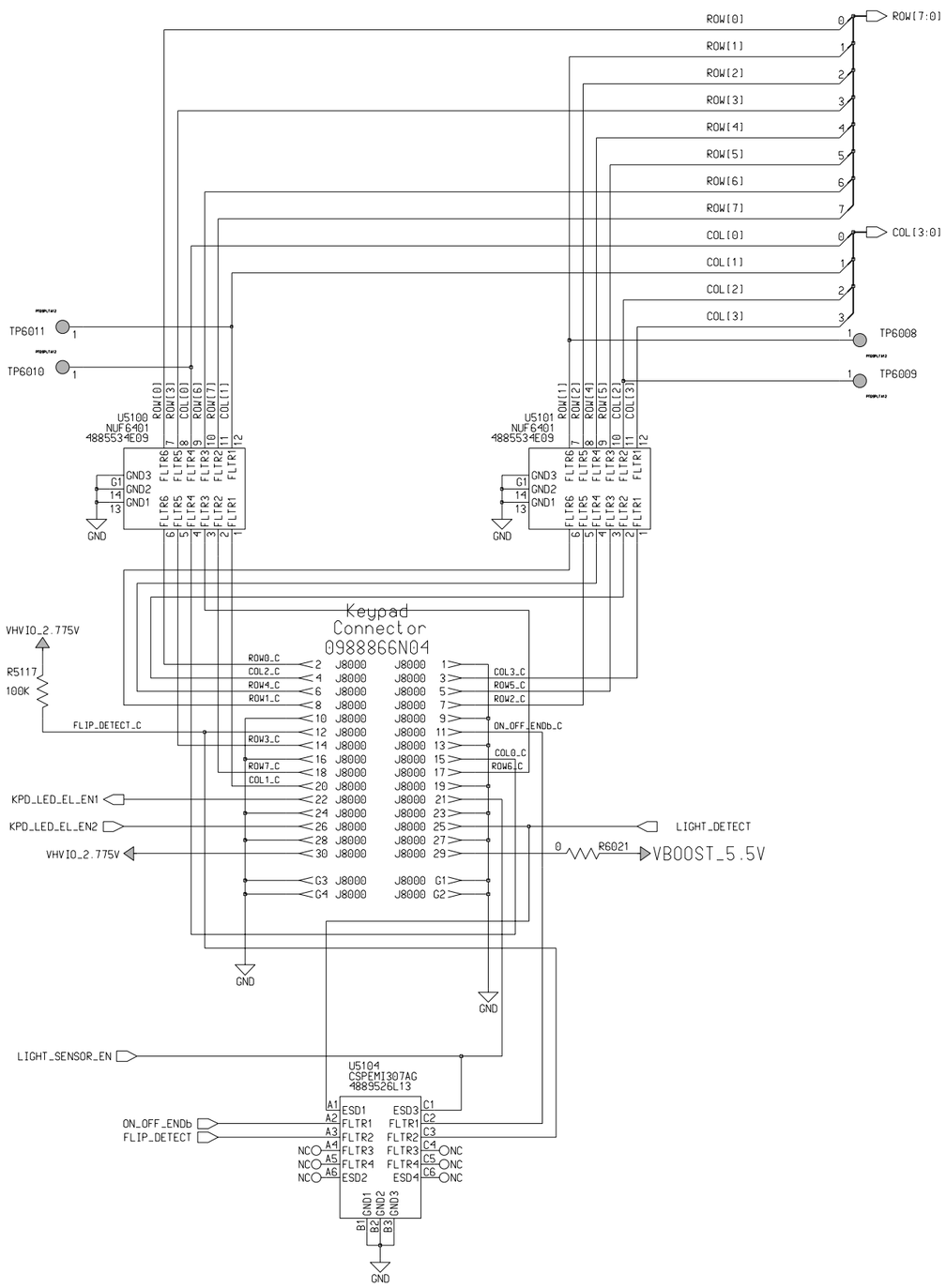
U1161

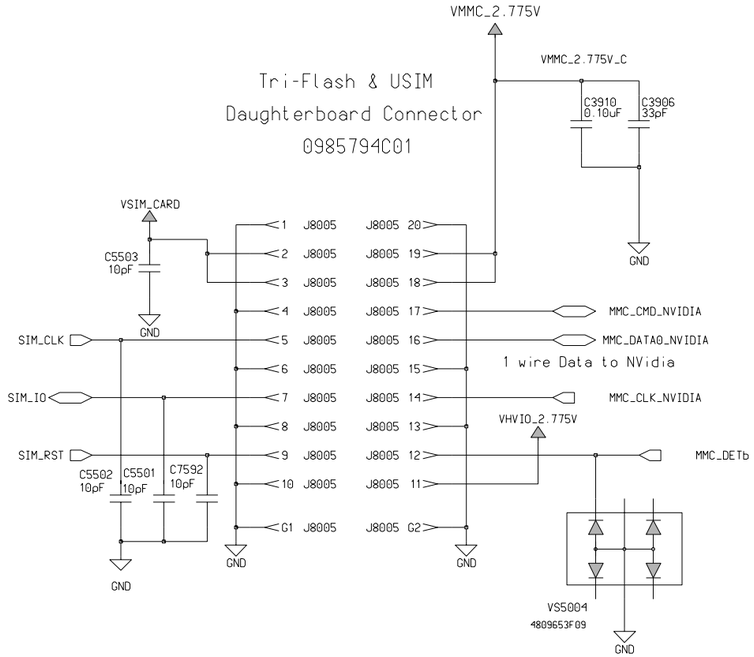
5114007M39
IN_A, IN_B, VCC, GND, OUT_Y
VLVIO_1.875V
NL17SZ08

NC, GPS_CLK

MOTOROLA CONFIDENTIAL PROPRIETARY

Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS IA Size:
DOC CTRL CHK:	SIM, Triflash, and Keypad Connectors
MFG CTRL CHK:	
QA CHK:	REV: P3 | Drawing Number: | Page: 3 | Of: 23
Changed by: frg025	Date: Thursday, March 31, 2005 | Time: 6:43:07 pm



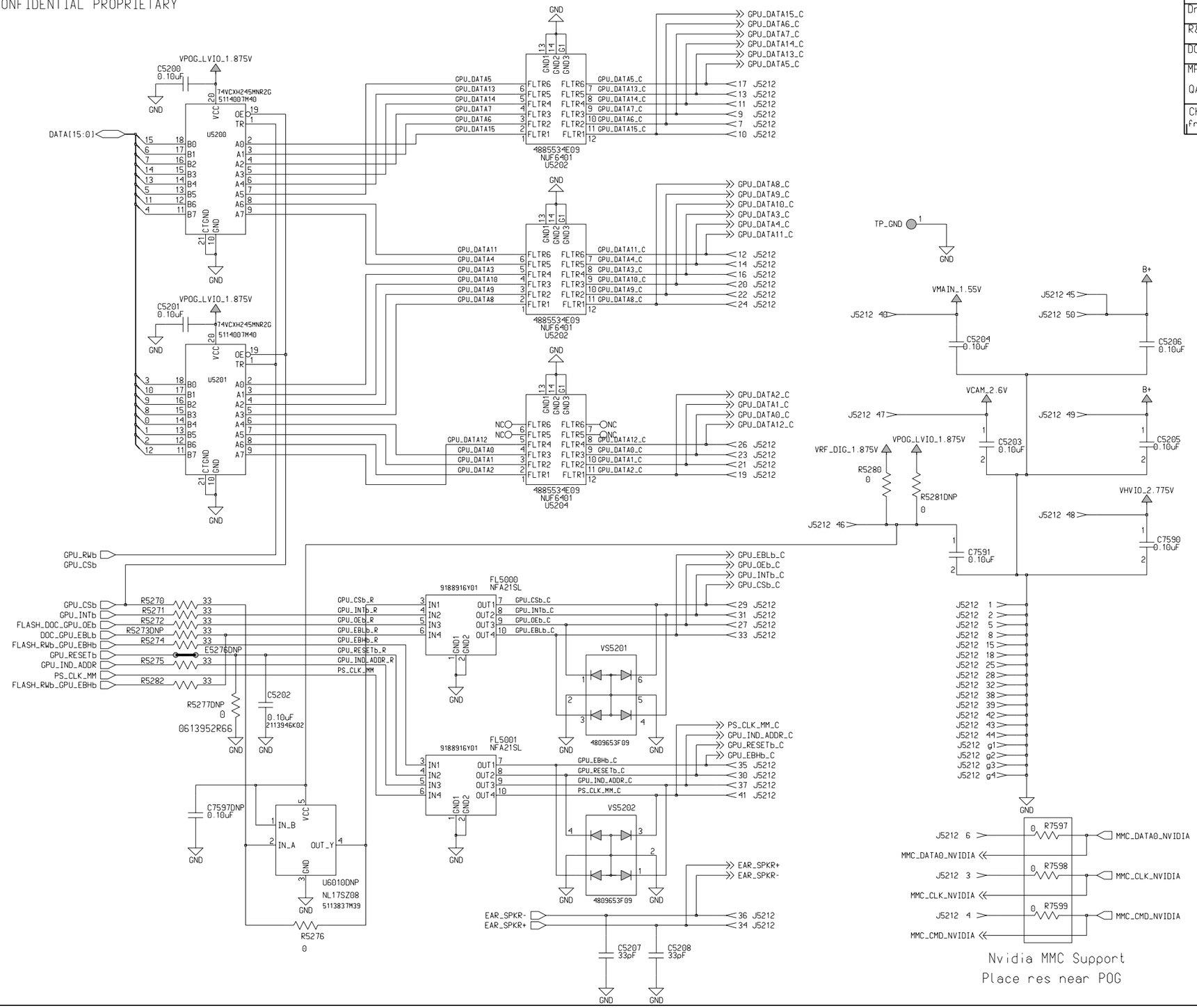


2 POLE IMPLEMENTATION FOR THE KEYPAD AND SIDE KEYS

	ROW7	ROW6	ROW5	ROW4	ROW3	ROW2	ROW1	ROW0
COL 0	6	4	2	8	*	#		9
COL 1	Left Soft	Menu	Right Soft	Carrier	Video Call Send	Voice Call Send		7
COL 2	Speaker	Vol Down	Vol Up	Camera	VR	0		5
COL 3	Nav Center	Nav Up	Nav Down	Nav Left	Nav Right	3	1	

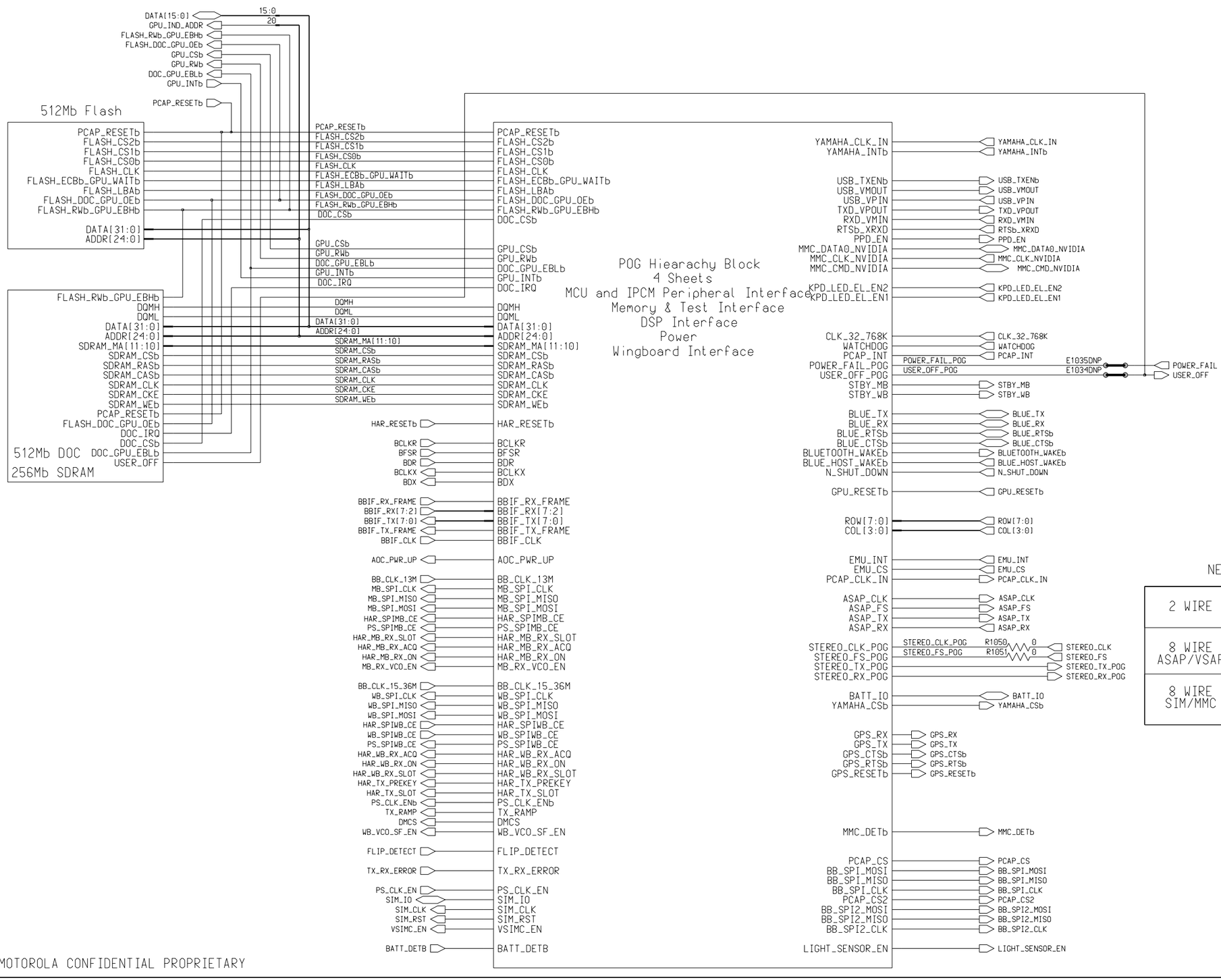
MOTOROLA CONFIDENTIAL PROPRIETARY

Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS IA — Size:
DOC CTRL CHK:	GPU & Flip Connector
MFG CTRL CHK:	REV: P3 — Drawing Number: — Page: 4 — Of: 23
QA CHK:	
Changed by: frg025	Date: Thursday, April 7, 2005 — Time: 4:47:34 pm



Nvidia MMC Support
Place res near POG

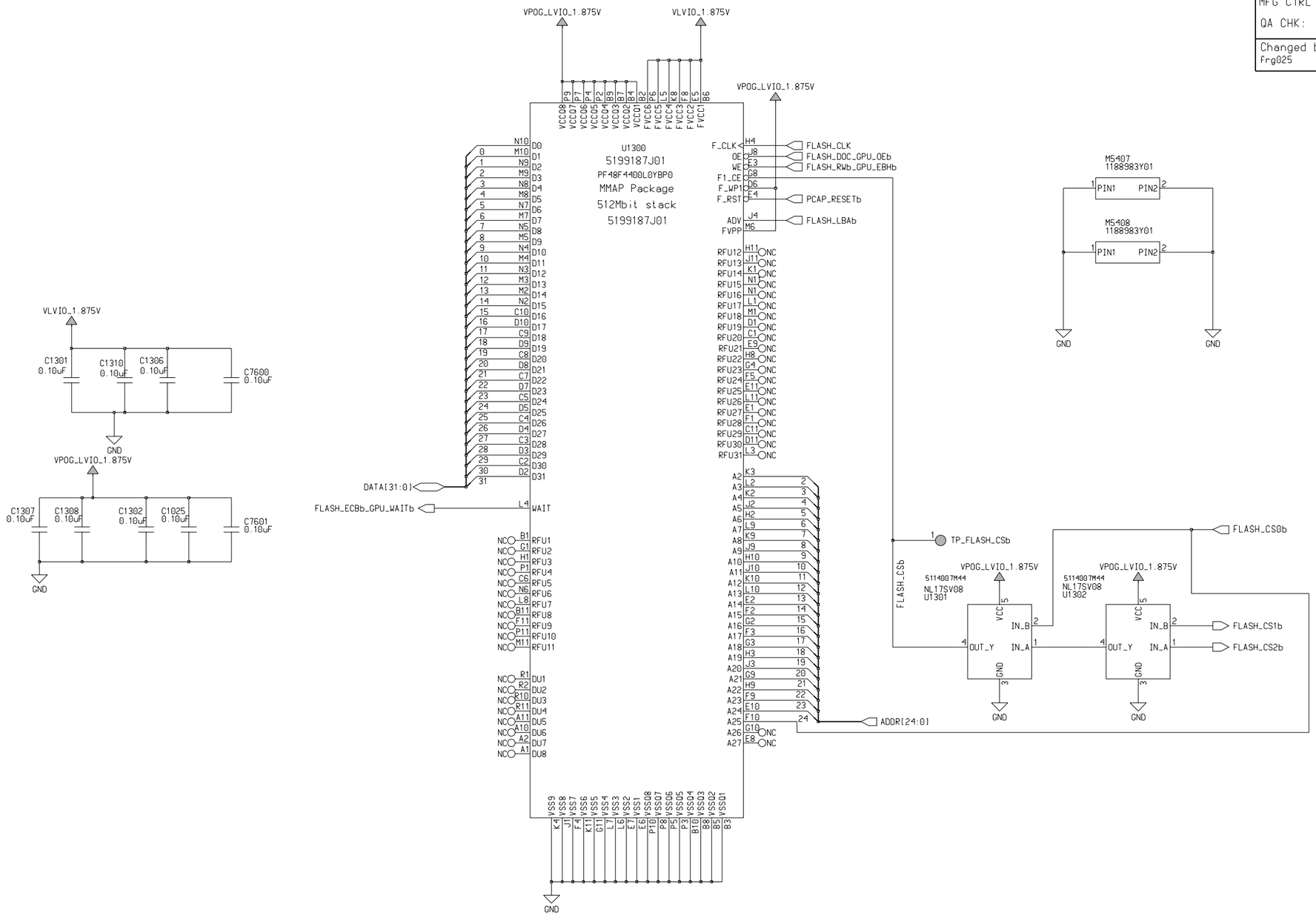
Engineer:	MOTOROLA INC.	
Drawn by:		
R&D CHK:	TITLE: SIRIUS IA POG & Memories	Size:
DOC CTRL CHK:		
MFG CTRL CHK:		
QA CHK:	REV: P3 | Drawing Number: | Page: 5 | Of: 23	
Changed by: frg025	Date: Tuesday, April 5, 2005	Time: 4:02:25 pm



NEXUS SETUP

2 WIRE	–
8 WIRE ASAP/VSAP	(UNSTACKED CORE) DNP R1050 DNP R1051
8 WIRE SIM/MMC	(PERIPH) DNP R1071 DNP R1072

Engineer:	MOTOROLA INC.		
Drawn by:			
R&D CHK:	TITLE: SIRIUS IA Flash Memory		Size:
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV: P3	Drawing Number:	Page: 6 Of: 23
Changed by: frg025	Date: Tuesday, March 29, 2005		Time: 6:52:37 pm



Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS IA SDRAM & DOC — Size:
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: P3 — Drawing Number: — Page: 7 — Of: 23
Changed by: frg025	Date: Wednesday, March 30, 2005 — Time: 6:04:52 pm

VLVIO_1.875V DOC_VCC VHVIO_2.775V
R5279DNP 0 R7581 0

VLVIO_1.875V C1402 0.10uF C1404 0.10uF C1405 0.10uF GND
DOC_VCC C6045 1.0uF C6041 .01uF C7599 0.10uF GND
VLVIO_1.875V C1406 0.10uF C1403 .01uF GND

SDRAM Supplies
K6 VCCQ
J6 VCC
DOC Supplies
G5 VCCQ
F1 VCC

R1402DNP 0
R1401DNP 0
R1400 0 GND
R1403DNP 0 USER_OFF

U6004 MS06D9SD8B3 5109509A71

SDRAM_CLK	C3	CLK_M	
	D7	CLK_SD	
DOC_CSb	E1	EN_CE	
FLASH_DOC_GPU_OEb	H3	EN_OE	
DOC_GPU_EBLb (R1406 0)	E2	EN_WE_M	
	C1	EN_WE_SD	
SDRAM_WEb	C5	CS	
SDRAM_CSb	D6	RAS	
SDRAM_RASb	E6	CAS	
SDRAM_CASb	E7	CKE	
SDRAM_CKE	C4	UDQM	
DQMH	D4	LDQM	
DQML	L5	LOCK	
R6022 0 PCAP_RESETb	G10	RSTIN	
ADDR[24:0] 13 14	E4	BA0	
	F4	BA1	
ADDR[24:0]	K1	A0_M	
	J1	A1_M	
	H1	A2_M	
	D1	A3_M	
	J2	A4_M	
	F3	A5_M	
	F5	A6_M	
	D5	A7_M	
	E3	A8_M	
	G6	A9_M	
	F9	A10_M	
	G9	A11_M	
ADDR[24:0]	D3	A12_M	
	D2	A0_SD	
	F2	A1_SD	
	G2	A2_SD	
	H2	A3_SD	
	H9	A4_SD	
	E9	A5_SD	
	D9	A6_SD	
	F8	A7_SD	
	E8	A8_SD	
SDRAM_MA[11:10]	D8	A9_SD	
	C2	A10_SD	
ADDR[24:0]	C8	A11_SD	
	F7	A12_SD	
NC	A1	NC1	
NC	L1	NC2	
NC	M1	NC3	
NC	A2	NC4	
NC	B2	NC5	
NC	K2	NC6	
NC	L2	NC7	
NC	M2	NC8	
NC	B3	NC9	
NC	L3	NC10	
NC	B4	NC11	
NC	L4	NC12	

VLVIO_1.875V VLVIO_1.875V DOC_VCC VLVIO_1.875V
VCC_SD_1 VCC_SD_2 VCC_M_1 VCC_M_2
J6 K6 F1 G5

R7582 10K R1405 10K VHVIO_2.775V

U6008 MC74VHC1GT50
5 VCC
2 IN_A
4 OUT_Y → DOC_IRQ
1 NC → NC
3 GND → GND

DMARQ	C1	NC
BUSY	E5	
IRQ	F6	
DQ0_SD	L6	DATA[31:0] 16
DQ1_SD	L7	17
DQ2_SD	L8	18
DQ3_SD	L9	19
DQ4_SD	K9	20
DQ5_SD	K10	21
DQ6_SD	J10	22
DQ7_SD	H10	23
DQ8_SD	E10	24
DQ9_SD	D10	25
DQ10_SD	C10	26
DQ11_SD	C9	27
DQ12_SD	B9	28
DQ13_SD	B8	29
DQ14_SD	B7	30
DQ15_SD	B6	31

DQ0_M	K3	DATA[31:0] 0
DQ1_M	J3	1
DQ2_M	G4	2
DQ3_M	H4	3
DQ4_M	K4	4
DQ5_M	J4	5
DQ6_M	H5	6
DQ7_M	K5	7
DQ8_M	H6	8
DQ9_M	K7	9
DQ10_M	J7	10
DQ11_M	G7	11
DQ12_M	H7	12
DQ13_M	K8	13
DQ14_M	J8	14
DQ15_M	H8	15

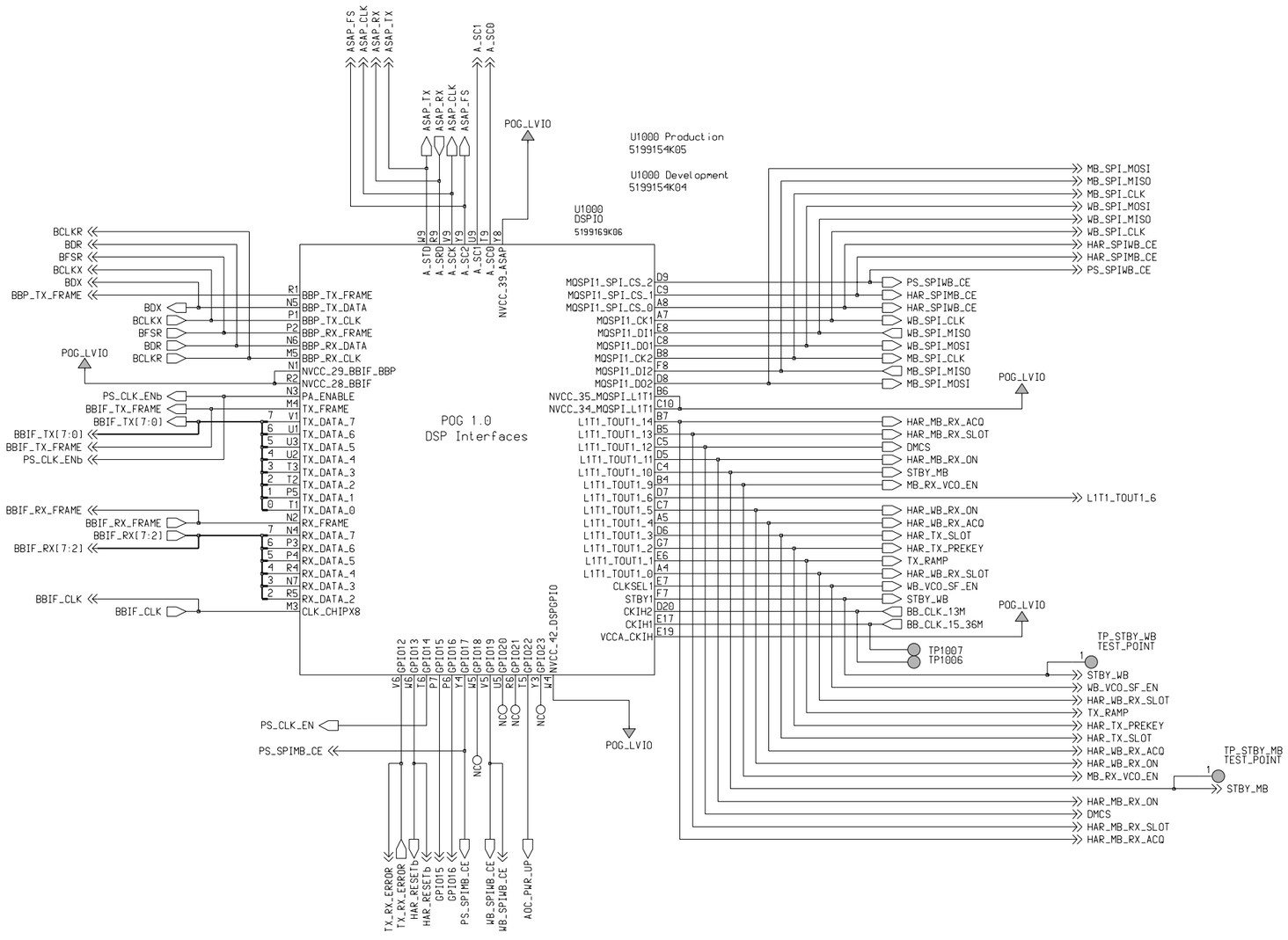
NC13	B5	NC
NC14	C5	NC
NC15	J5	NC
NC16	A9	NC
NC17	M9	NC
NC18	A10	NC
NC19	B10	NC
NC20	F10	NC
NC21	L10	NC
NC22	M10	NC

VSS1 VSS2 VSS3 VSS4
G1 G3 G8 J9
GND

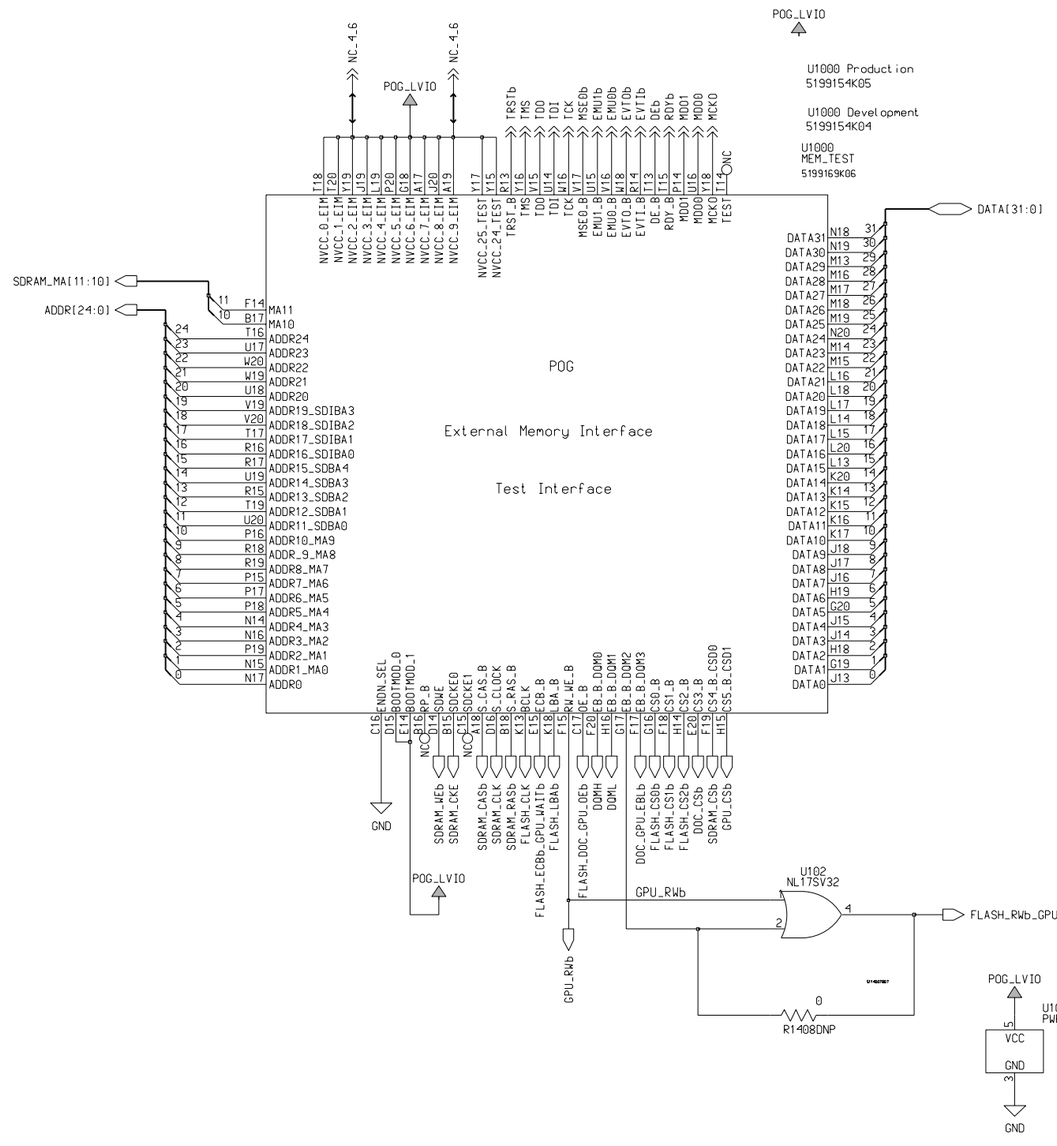
M5405 1188983Y01 PIN1 PIN2 GND
M5406 1188983Y01 PIN1 PIN2 GND

MOTOROLA CONFIDENTIAL PROPRIETARY

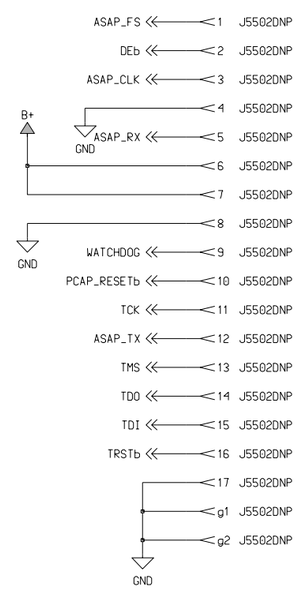
Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS IA — Size:
DOC CTRL CHK:	POG DSP Interface
MFG CTRL CHK:	
QA CHK:	REV: P3 — Drawing Number: — Page: 8 — Of: 23
Changed by: e11248	Date: Monday, February 28, 2005 — Time: 3:55:21 pm



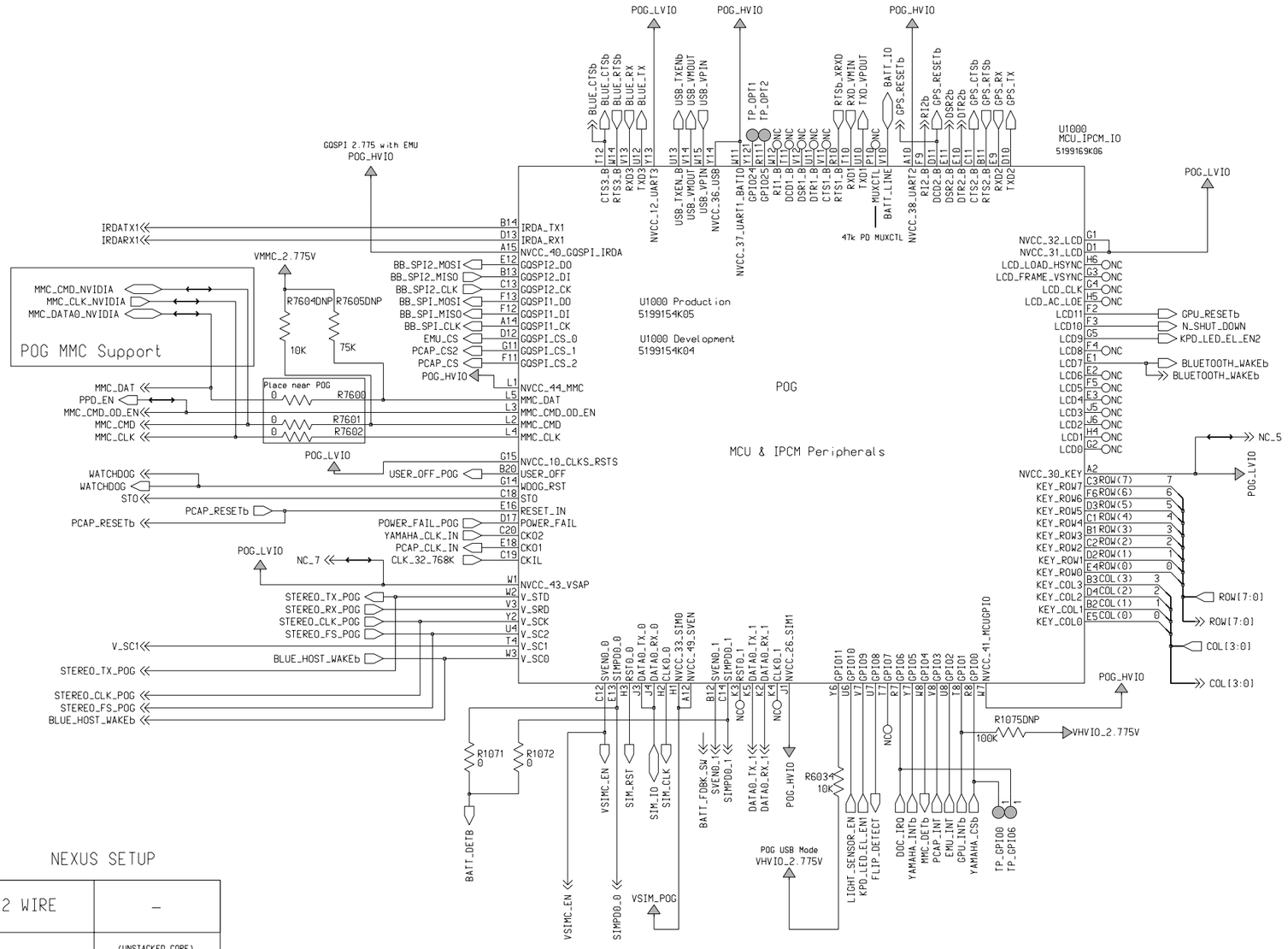
Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS IA Size:
DOC CTRL CHK:	
MFG CTRL CHK:	POG Memory & Test Interface
QA CHK:	REV: P3 | Drawing Number: | Page: 9 | Of: 23
Changed by: frg025	Date: Tuesday, April 5, 2005 | Time: 3:54:41 pm



JTAG CONNECTOR
17 pin ZIF
0988248Y01



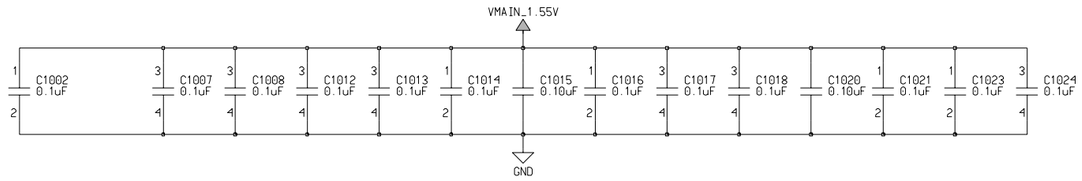
Engineer:	MOTOROLA INC.		
Drawn by:			
R&D CHK:	TITLE: SIRIUS IA		Size:
DOC CTRL CHK:	POG Peripheral Int		
MFG CTRL CHK:			
QA CHK:	REV: P3	Drawing Number:	Page: 10 Of: 23
Changed by: frg025	Date: Tuesday, April 5, 2005		Time: 3:56:41 pm

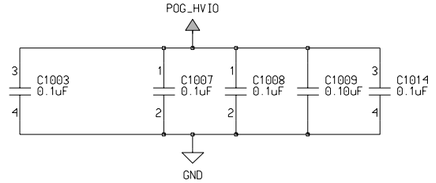


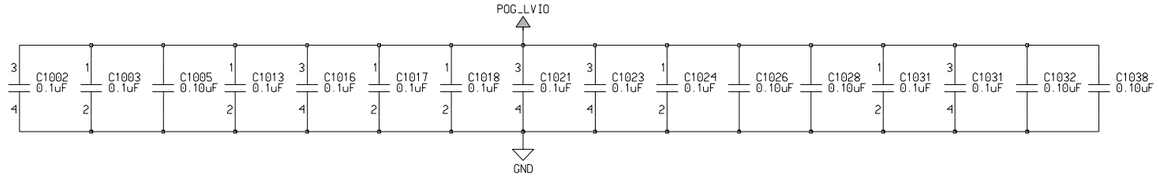
NEXUS SETUP

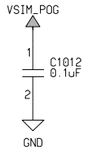
2 WIRE	–
8 WIRE ASAP/VSAP	(UNSTACKED CORE) DNP R1050 DNP R1051
8 WIRE SIM/MMC	(PERIPH) DNP R1071 DNP R1072

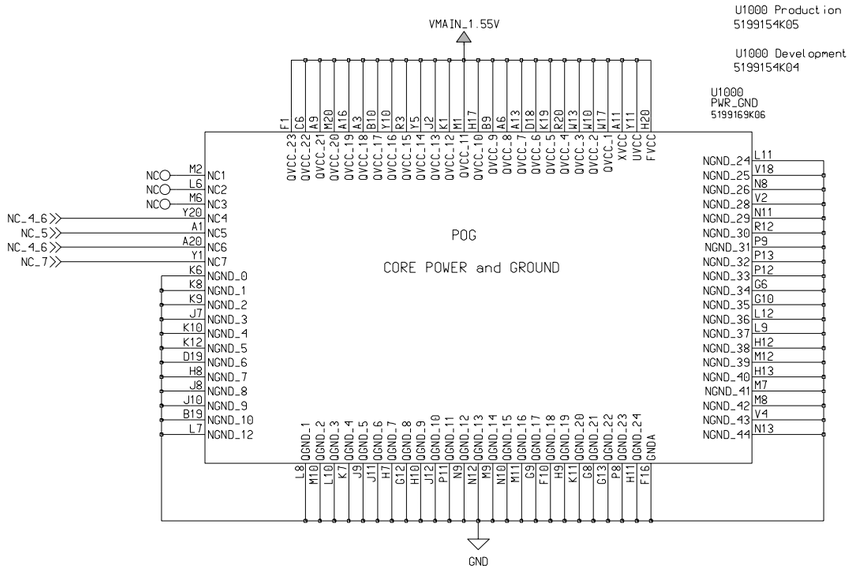
Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS POG Power Interface — Size:
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: P3 — Drawing Number: — Page: 11 — Of: 23
Changed by: frg025	Date: Tuesday, April 5, 2005 — Time: 3:57:24 pm

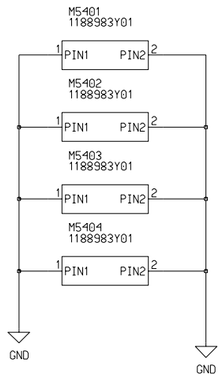




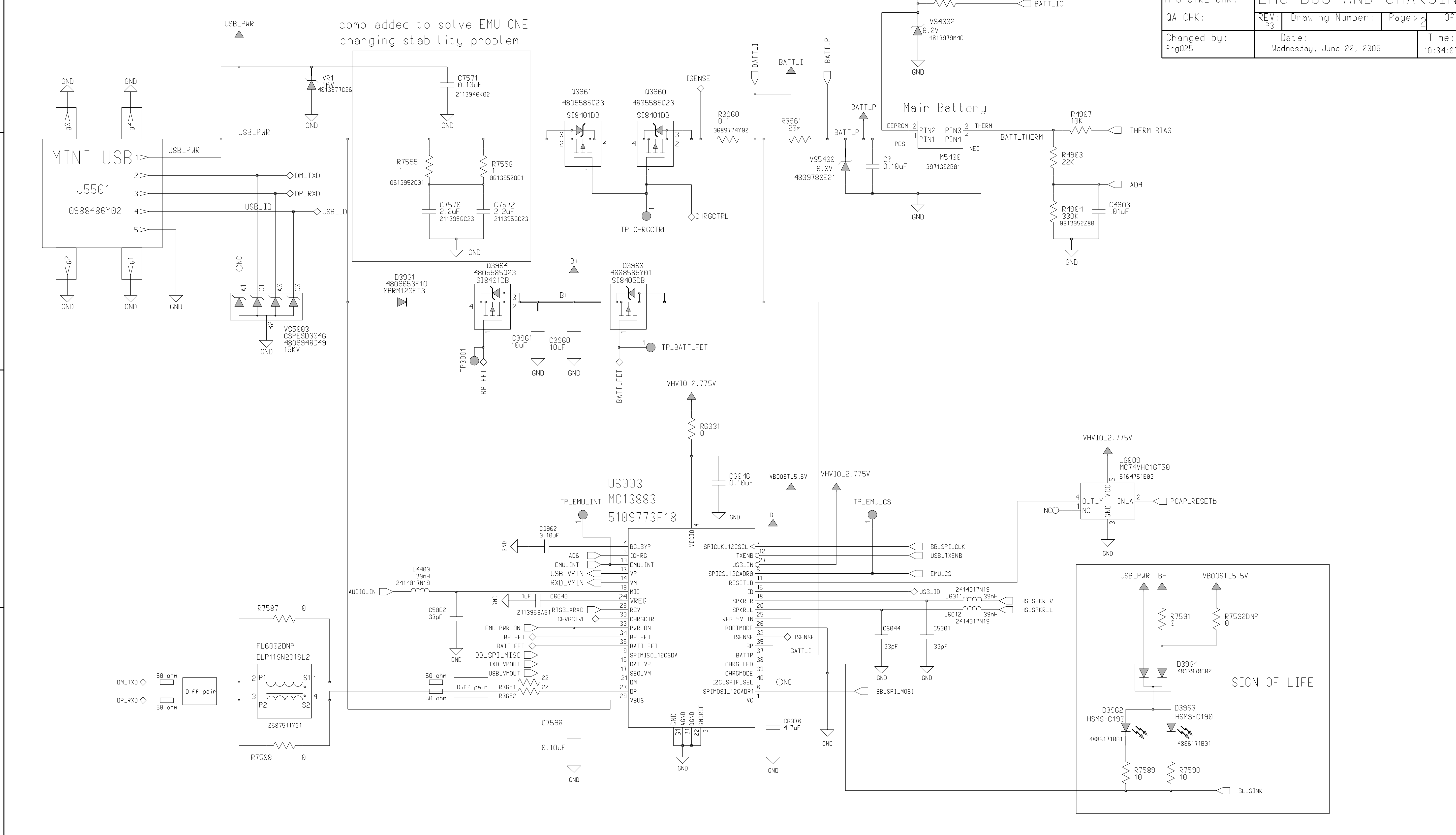








MOTOROLA CONFIDENTIAL PROPRIETARY

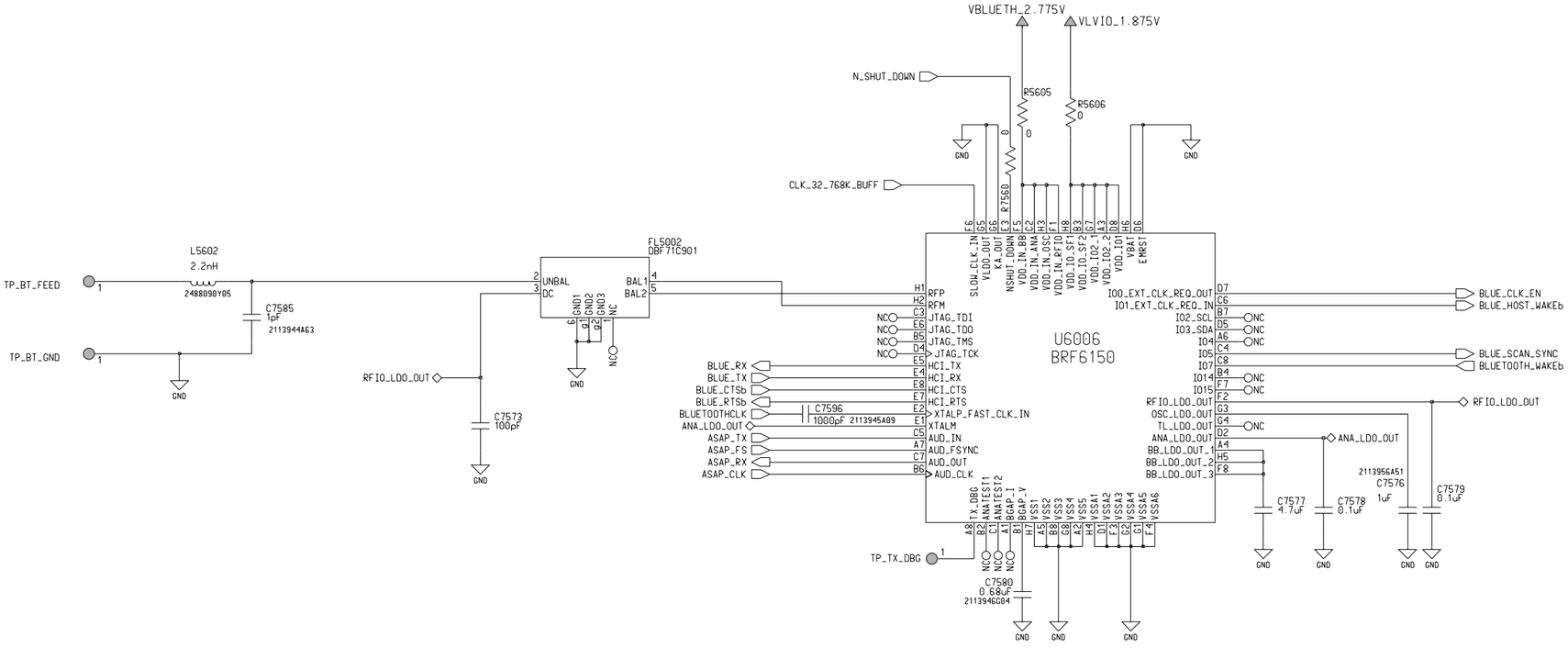


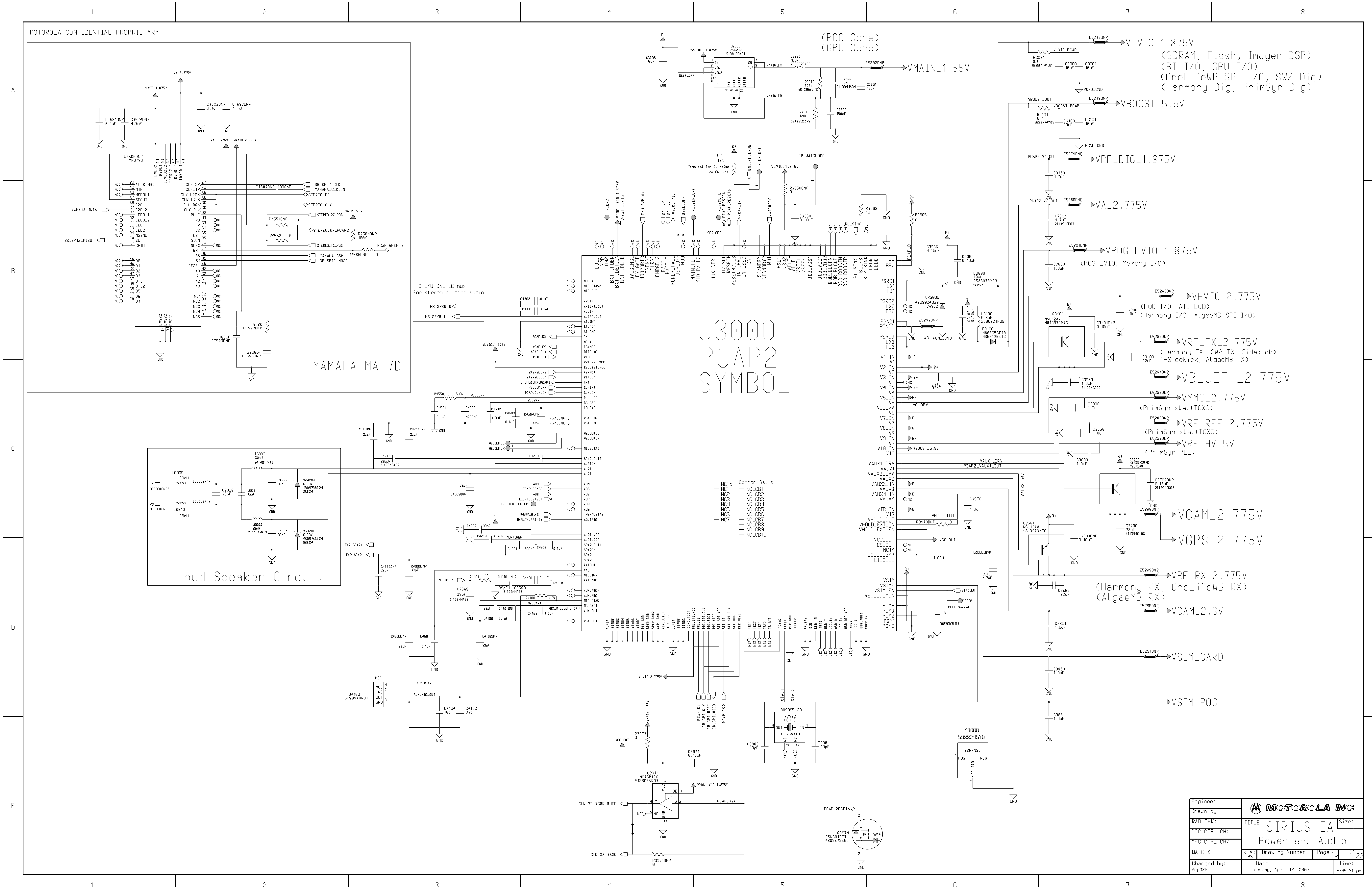
comp added to solve EMU ONE charging stability problem
MINI USB
J5501
0988486Y02
USB_PWR
DM_TXD
DP_RXD
USB_ID
GND
VR1 16V 4813977C26
C7571 0.10uF 2113946K02
R7555 1 0613952Q01
R7556 1 0613952Q01
C7570 2.2uF 2113956C23
C7572 2.2uF 2113956C23
VS5003 CSPESD304G 4809948D49 15KV
NC
Q3961 4805585Q23 SI8401DB
Q3960 4805585Q23 SI8401DB
ISENSE
TP_CHRGCTRL
CHRGCTRL
R3960 0.1 0689774Y02
BATT_I
BATT_P
R3961 20m
VS5400 6.8V 4809788E21
C? 0.10uF
Main Battery
EEPROM
PIN2 PIN1 PIN3 PIN4
POS
NEG
THERM
M5400 3971392B01
VHVIO_2.775V
R5401 4.7K
R5402 100
BATT_IO
VS4302 6.2V 4813979M40
R4907 10K
THERM_BIAS
BATT_THERM
R4903 22K
AD4
R4904 330K 0613952Z80
C4903 .01uF
NC PPD_EN
D3961 4809653F10 MBRM120ET3
Q3964 4805585Q23 SI8401DB
B+
Q3963 4888585Y01 SI8405DB
C3961 10uF
C3960 10uF
TP3001
BP_FET
TP_BATT_FET
BATT_FET
R6031 0
C6046 0.10uF
U6003
MC13883
5109773F18
TP_EMU_INT
TP_EMU_CS
VBOOST_5.5V
C3962 0.10uF
AD6
EMU_INT
USB_VPIN
RXD_VMIN
AUDIO_IN
L4400 39nH 2414017N19
C5002 33pF
1uF C6040 2113956A51
RTSB_XRXD
EMU_PWR_ON
BB_SPI_MISO
TXD_VPOUT
USB_VMOUT
R3651 22
R3652 22
C7598 0.10uF
BG_BYP ICHRG EMU_INT VP VM MIC VREG RCV CHRGCTRL PWR_ON BP_FET BATT_FET SPIMISO_12CSDA DAT_VP SE0_VM DM DP VBUS
VCCIO
SPICLK_12CSCL TXENB USB_EN SPICS_12CADR0 RESET_B ID SPKR_R SPKR_L REG_5V_IN BOOTMODE ISENSE BP BATTP CHRG_LED CHRGMODE I2C_SPIF_SEL SPIMOSI_12CADR1 VC
GND AGND DGND GNDREF
C6038 4.7uF
BB_SPI_CLK
USB_TXENB
EMU_CS
L6011 39nH 2414017N19
L6012 39nH 2414017N19
HS_SPKR_R
HS_SPKR_L
C6044 33pF
C5001 33pF
BB_SPI_MOSI
U6009 MC74VHC1GT50 5164751E03
OUT_Y NC VCC GND IN_A
PCAP_RESETb
R7587 0
R7588 0
FL6002DNP
DLP11SN201SL2
2587511Y01
50 ohm
Diff pair
USB_PWR B+ VBOOST_5.5V
R7591 0
R7592DNP 0
D3964 4813978C02
SIGN OF LIFE
D3962 HSMS-C190 4886171B01
D3963 HSMS-C190 4886171B01
R7589 10
R7590 10
BL_SINK

Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS IA
DOC CTRL CHK:	EMU BUS AND CHARGING
MFG CTRL CHK:	
QA CHK:	REV: P3 · Drawing Number: · Page: 12 · Of: 23
Changed by: frg025	Date: Wednesday, June 22, 2005 · Time: 10:34:07 am

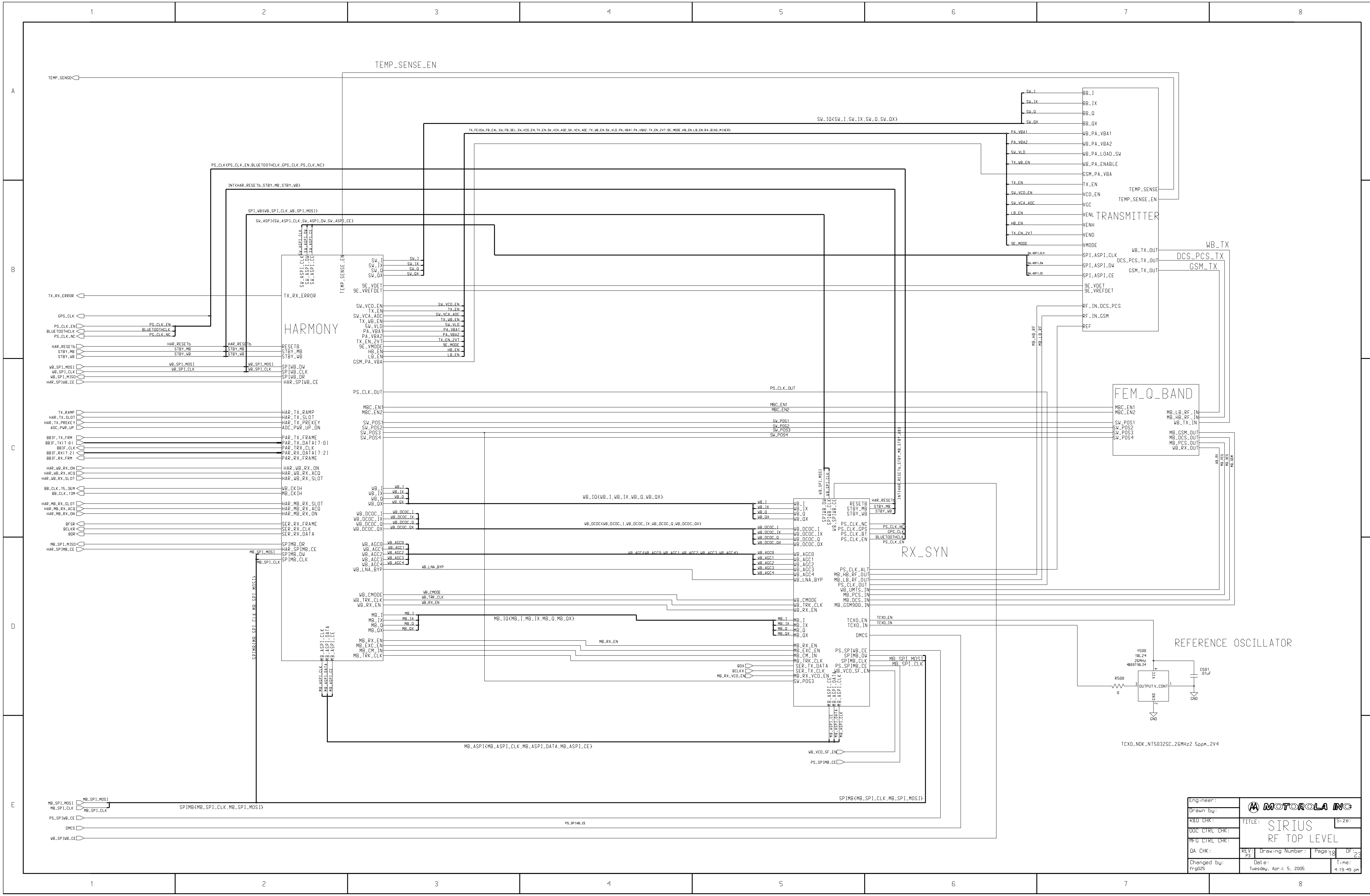
Engineer:	MOTOROLA INC.	
Drawn by:		
R&D CHK:	TITLE: SIRIUS Bluetooth	Size:
DOC CTRL CHK:		
MFG CTRL CHK:		
QA CHK:	REV: P3 | Drawing Number: | Page: 14 | Of: 23	
Changed by: frg025	Date: Tuesday, April 5, 2005	Time: 4:08:48 pm

Connect to POG PERIPH:F3 (LCD10)





MOTOROLA CONFIDENTIAL PROPRIETARY
YAMAHA MA-7D
U3500DNP
YMU790
VA_2.775V
VLVIO_1.875V
VHVIO_2.775V
BB_SPI2_CLK
YAMAHA_CLK_IN
STEREO_FS
STEREO_CLK
STEREO_RX_POG
STEREO_RX_PCAP2
STEREO_TX_POG
YAMAHA_CSb
BB_SPI2_MOSI
BB_SPI2_MISO
YAMAHA_INTb
PCAP_RESETb
TO EMU ONE IC mux
for stereo or mono audio
HS_SPKR_R
HS_SPKR_L
Loud Speaker Circuit
LOUD_SPK-
LOUD_SPK+
EAR_SPKR+
EAR_SPKR-
AUDIO_IN
MIC
J4100
5089874N01
MIC_BIAS
AUX_MIC_OUT
(POG Core)
(GPU Core)
U3200
TPS62021
5188128Y01
VMAIN_1.55V
TP_WATCHDOG
Temp sol for EL noise on ON line
U3000
PCAP2
SYMBOL
Corner Balls
VLVIO_1.875V
(SDRAM, Flash, Imager DSP)
(BT I/O, GPU I/O)
(OneLifeWB SPI I/O, SW2 Dig)
(Harmony Dig, PrimSyn Dig)
VBOOST_5.5V
VRF_DIG_1.875V
VA_2.775V
VPOG_LVIO_1.875V
(POG LVIO, Memory I/O)
VHVIO_2.775V
(POG I/O, ATI LCD)
(Harmony I/O, AlgaeMB SPI I/O)
VRF_TX_2.775V
(Harmony TX, SW2 TX, Sidekick)
(HSidekick, AlgaeMB TX)
VBLUETH_2.775V
VMMC_2.775V
(PrimSyn xtal+TCXO)
VRF_REF_2.775V
(PrimSyn xtal+TCXO)
VRF_HV_5V
(PrimSyn PLL)
VCAM_2.775V
VGPS_2.775V
VRF_RX_2.775V
(Harmony RX, OneLifeWB RX)
(AlgaeMB RX)
VCAM_2.6V
VSIM_CARD
VSIM_POG
M3000
5988245Y01
SSR-N9L
U3971
NC7SP126
5188085K07
CLK_32_768K_BUFF
CLK_32_768K
PCAP_32K
Y3982
MC146
32.768KHz
Q3974
2SK3019FTL
4809579E67
Engineer:
Drawn by:
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:
QA CHK:
MOTOROLA INC
TITLE: SIRIUS IA
Power and Audio
Size:
REV: P3
Drawing Number:
Page: 15
Of: 23
Changed by: frg025
Date: Tuesday, April 12, 2005
Time: 5:45:31 pm



Engineer:
Drawn by:
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:
QA CHK:
Changed by: frg025

MOTOROLA INC

TITLE: SIRIUS RF TOP LEVEL

Size:

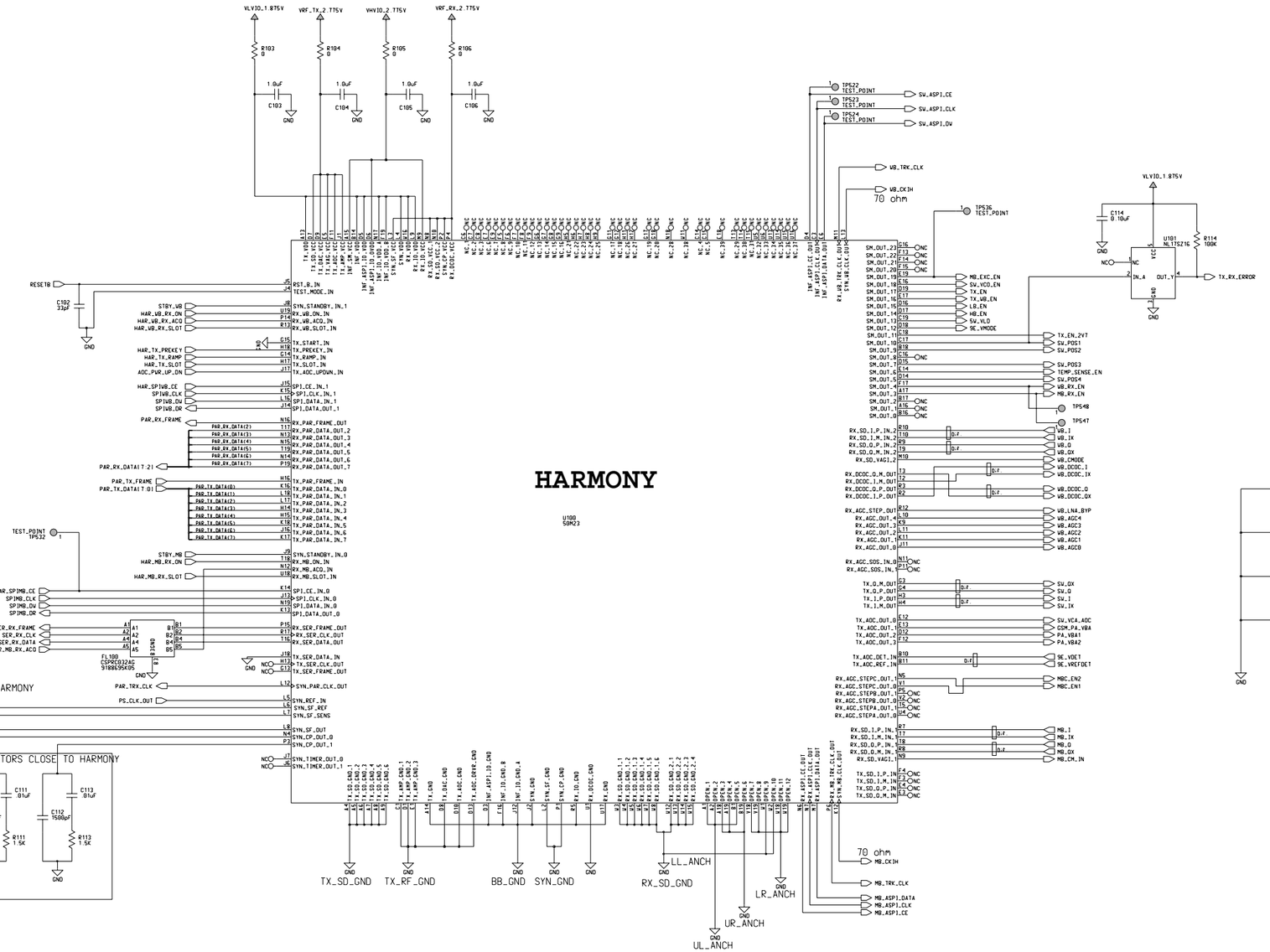
REV: P3 | Drawing Number: | Page: 18 | Of: 23

Date: Tuesday, April 5, 2005 | Time: 4:19:49 pm

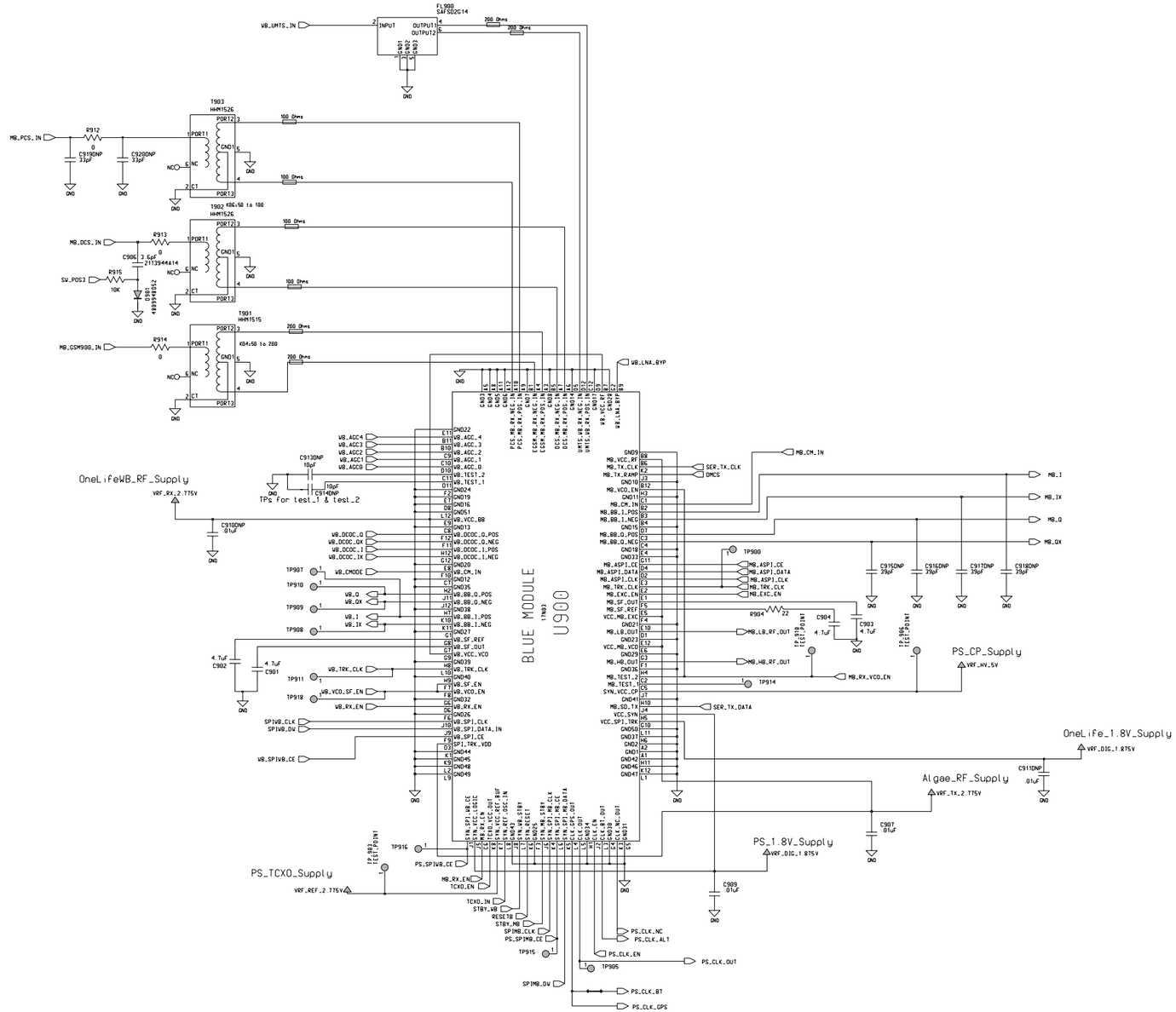
TP placeholders for pins with NC

SYNTHESIS CAPACITORS CLOSE TO HARMONY

SUPPLIES INTERCONNECTIONS FAR FROM HARMONY



Engineer:	MOTOROLA INC
Drawn by:	
R&D CHK:	TITLE: SIRIUS HARMONY
DOC CTRL CHK:	Size:
MFG CTRL CHK:	
QA CHK:	REV: P3 Drawing Number: Page: 19 OF: 23
Changed by: frg025	Date: Tuesday, April 5, 2005 Time: 4:15:58 pm



Changed by frg025	Date Changed Tuesday, April 5, 2005	Time 4:19:02 pm	QA CHK	REV 1.0	Drawing Number	Sheet 20 of 23	

Engineer Matt Schneider	MOTOROLA
Drawn by Matt Schneider	BOYNTON BEACH FLORIDA
R&D CHK	TITLE: SIRIUS Rx/Syn — Size D
DOC CTRL CHK	
MFG CTRL CHK	

GSM/DCS/PCS and WCDMA Transmitters

TX_RATTLER _MODULE

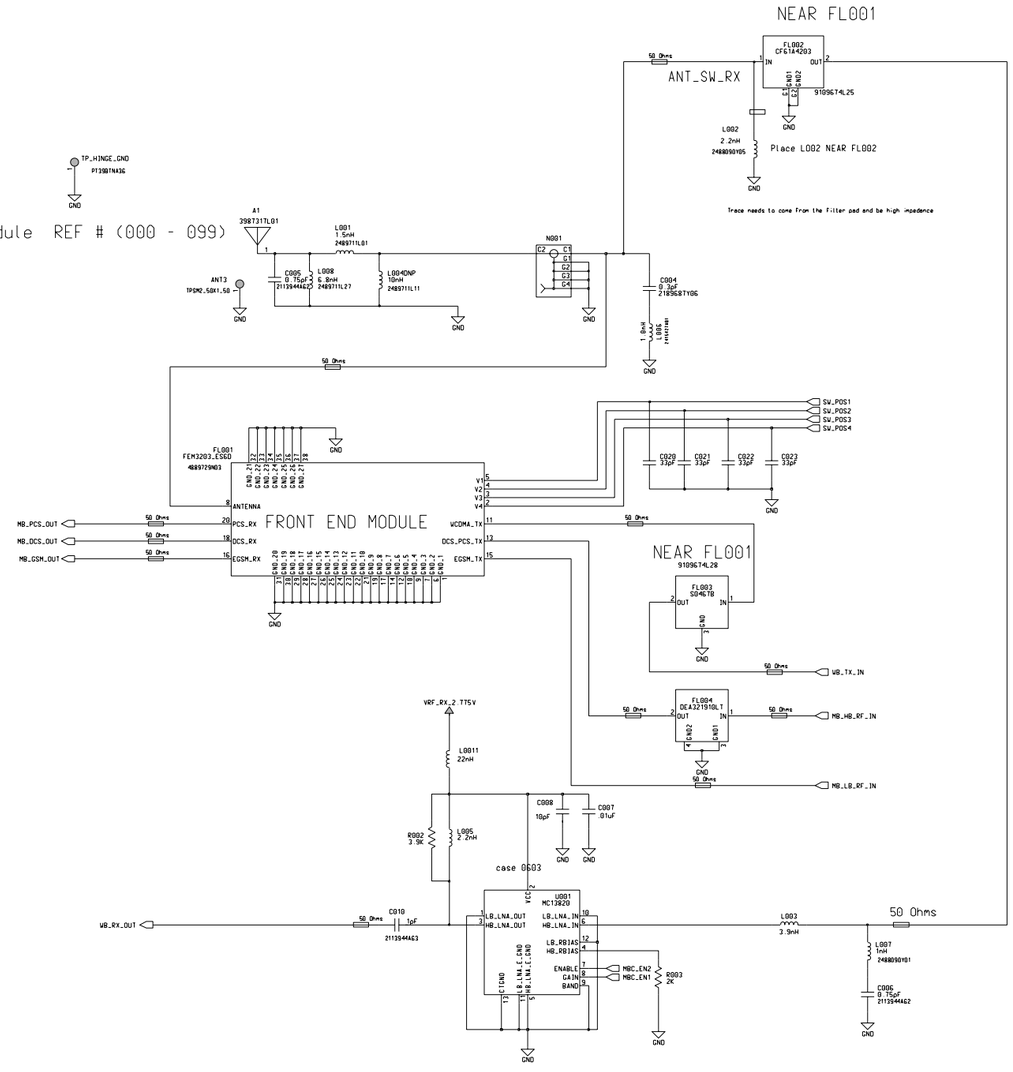
GSM/DCS/PCS PA REF# (800 - 829)

Temp Sensor REF # (880 - 889)

WCDMA PA REF # (850 - 879)

Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: SIRIUS IA TRANSMITTER
DOC CTRL CHK:	Size:
MFG CTRL CHK:	
QA CHK:	REV: P3 | Drawing Number: | Page: 21 OF: 23
Changed by: frg025	Date: Tuesday, April 5, 2005 | Time: 4:17:06 pm

Front End Module REF # (000 - 099)



Engineer:	MOTOROLA INC
Drawn by:	
R&D CHK:	TITLE: SIRIUS Size:
DOC CTRL CHK:	Quad Band Front End Module
MFG CTRL CHK:	
QA CHK:	REV: P3 Drawing Number: Page 22 OF 23
Changed by: frg025	Date: Tuesday, April 5, 2005 Time: 4:18:02 pm