Single-Phase Multifunction Metering IC with di/dt Sensor Interface

ADE7753

FEATURES

High accuracy; supports IEC 61036/61827 and IEC61268
On-chip digital integrator enables direct interface to current sensors with di/dt output
Active, reactive, and apparent energy; sampled waveform; current and voltage RMS
Less than 0.1% error in active energy measurement over a dynamic range of 1000 to 1 at 25°C
Positive-only energy accumulation mode available
On-chip user programmable threshold for line voltage surge and SAG and PSU supervisory
Digital calibration for power, phase, and input offset
On-chip temperature sensor (±3°C typical)
SPI® compatible serial interface
Pulse output with programmable frequency
Interrupt request pin ($\overline{\text{IRQ}}$) and status register
Reference 2.4 V with external overdrive capability
Single 5 V supply, low power (25 mW typical)

GENERAL DESCRIPTION

The ADE7753 features proprietary ADCs and DSP for high accuracy over large variations in environmental conditions and time. The ADE7753 incorporates two second order 16-bit Σ-Δ ADCs, a digital integrator (on CH1), reference circuitry, temperature sensor, and all the signal processing required to perform active, reactive, and apparent energy measurements, line-voltage period measurement, and RMS calculation on the voltage and current. The selectable on-chip digital integrator provides direct interface to di/dt current sensors such as Rogowski coils, eliminating the need for an external analog integrator and resulting in excellent long-term stability and precise phase matching between the current and voltage channels.

The ADE7753 provides a serial interface to read data, and a pulse output frequency (CF), which is proportional to the active power. Various system calibration features, i.e., channel offset correction, phase calibration, and power calibration, ensure high accuracy. The part also detects short duration low or high voltage variations.

The positive-only accumulation mode gives the option to accumulate energy only when positive power is detected. An internal no-load threshold ensures that the part does not exhibit any creep when there is no load. The zero-crossing output (ZX) produces a pulse that is synchronized to the zero-crossing point of the line voltage. This signal is used internally in the line cycle active and apparent energy accumulation modes, which enables faster calibration.

The interrupt status register indicates the nature of the interrupt, and the interrupt enable register controls which event produces an output on the $\overline{\text{IRQ}}$ pin, an open-drain, active low logic output.

The ADE7753 is available in a 20-lead SSOP package.

FUNCTIONAL BLOCK DIAGRAM

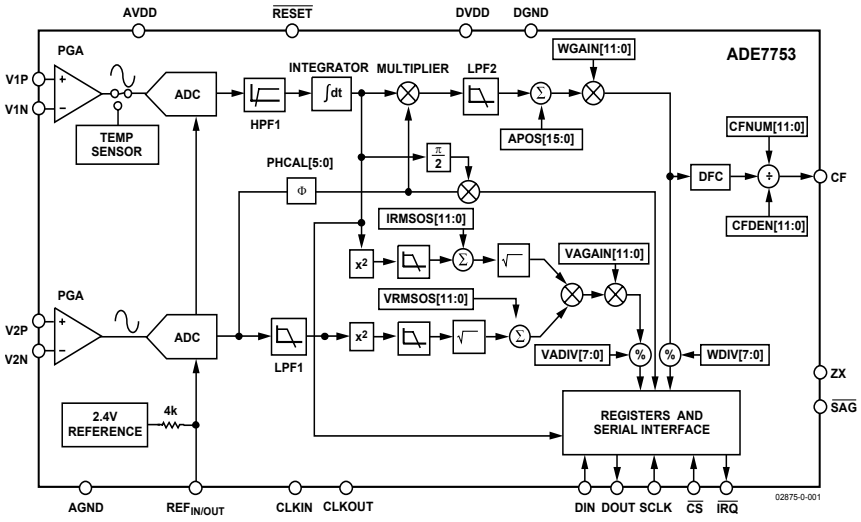

Figure 1. ADE7753 Functional Block Diagram

*U.S. Patents 5,745,323; 5,760,617; 5,862,069; 5,872,469; Others Pending

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

ADE7753–SPECIFICATIONS[1, 2]

Table 1. (AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 3.579545 MHz XTAL, T_{MIN} to T_{MAX} = −40°C to +85°C)

Parameter	Spec	Unit	Test Conditions/Comments
ENERGY MEASUREMENT ACCURACY			
Active Power Measurement Error			CLKIN = 3.579545 MHz
Channel 1 Range = 0.5 V Full Scale			Channel 2 = 300 mV rms/60 Hz, Gain = 2
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.1	% typ	Over a dynamic range 1000 to 1
Channel 1 Range = 0.25 V Full Scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.2	% typ	Over a dynamic range 1000 to 1
Channel 1 Range = 0.125 V Full Scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.2	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.2	% typ	Over a dynamic range 1000 to 1
Active Power Measurement Bandwidth	14	kHz	
Phase Error 1 between Channels	±0.05	max	Line Frequency = 45 Hz to 65 Hz, HPF on
AC Power Supply Rejection[1]			AV_{DD} = DV_{DD} = 5 V + 175 mV rms/120 Hz
Output Frequency Variation (CF)	0.2	% typ	Channel 1 = 20 mV rms, Gain = 16, Range = 0.5 V Channel 2 = 300 mV rms/60 Hz, Gain = 1
DC Power Supply Rejection[1]			AV_{DD} = DV_{DD} = 5 V ± 250 mV dc
Output Frequency Variation (CF)	±0.3	% typ	Channel 1 = 20 mV rms/60 Hz, Gain = 16, Range = 0.5 V Channel 2 = 300 mV rms/60 Hz, Gain = 1
I_{rms} Measurement Error	0.5	% typ	Over a dynamic range 100 to 1
I_{rms} Measurement Bandwidth	14	kHz	
V_{rms} Measurement Error	0.5	% typ	Over a dynamic range 20 to 1
V_{rms} Measurement Bandwidth	140	Hz	
ANALOG INPUTS[3]			See Analog Inputs section
Maximum Signal Levels	±0.5	V max	V1P, V1N, V2N, and V2P to AGND
Input Impedance (dc)	390	k min	
Bandwidth	14	kHz	CLKIN/256, CLKIN = 3.579545 MHz
Gain Error[1,3]			External 2.5 V reference, Gain = 1 on Channels 1 and 2
Channel 1			
Range = 0.5 V Full Scale	±4	% typ	V1 = 0.5 V dc
Range = 0.25 V Full Scale	±4	% typ	V1 = 0.25 V dc
Range = 0.125 V Full Scale	±4	% typ	V1 = 0.125 V dc
Channel 2	±4	% typ	V2 = 0.5 V dc
Offset Error 1	±32	mV max	Gain 1
Channel 1	±13	mV max	Gain 16
	±32	mV max	Gain 1
Channel 2	±13	mV max	Gain 16
WAVEFORM SAMPLING			Sampling CLKIN/128, 3.579545 MHz/128 = 27.9 kSPS
Channel 1			See Channel 1 Sampling section
Signal-to-Noise Plus Distortion	62	dB typ	150 mV rms/60 Hz, Range = 0.5 V, Gain = 2
Bandwidth(−3 dB)	14	kHz	CLKIN = 3.579545 MHz

Parameter	Spec	Unit	Test Conditions/Comments
Channel 2			See Channel 2 Sampling
Signal-to-Noise Plus Distortion	60	dB typ	150 mV rms/60 Hz, Gain = 2
Bandwidth (–3 dB)	140	Hz	CLKIN = 3.579545 MHz
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.6	V max	2.4 V + 8%
	2.2	V min	2.4 V – 8%
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.4 V at $REF_{IN/OUT}$ pin
Reference Error	±200	mV max	
Current source	10	µA max	
Output Impedance	3.4	kΩ min	
Temperature Coefficient	30	ppm/°C typ	
CLKIN			All specifications CLKIN of 3.579545 MHz
Input Clock Frequency	4	MHz max	
	1	MHz min	
LOGIC INPUTS			
$\overline{RESET}$, DIN, SCLK, CLKIN, and $\overline{CS}$			
Input High Voltage, V_{INH}	2.4	V min	DV_{DD} = 5 V ± 10%
Input Low Voltage, V_{INL}	0.8	V max	DV_{DD} = 5 V ± 10%
Input Current, I_{IN}	±3	µA max	Typically 10nA, V_{IN} = 0 V to DV_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS			
$\overline{SAG}$ and $\overline{IRQ}$			Open-drain outputs, 10 kΩ pull-up resistor
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
ZX and DOUT			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
CF			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	1	V max	I_{SINK} = 7 mA
POWER SUPPLY			For specified performance
AV_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
DV_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
AI_{DD}	3	mA max	Typically 2.0 mA
DI_{DD}	4	mA max	Typically 3.0 mA

[1]See Terminology section for explanation of specifications.
[2]See plots in Typical Performance Characteristics.
[3]See Analog Inputs section.

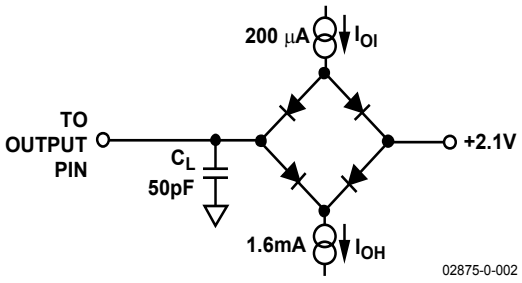

Figure 2. Load Circuit for Timing Specifications

ADE7753–TIMING CHARACTERISTICS[1, 2]

Table 2. (AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 3.579545 MHz XTAL, T_{MIN} to T_{MAX} = −40°C to +85°C)

Parameter	Spec	Unit	Test Conditions/Comments
Write Timing			
t_1	50	ns (min)	$\overline{CS}$ falling edge to first SCLK falling edge.
t_2	50	ns (min)	SCLK logic high pulse width.
t_3	50	ns (min)	SCLK logic low pulse width.
t_4	10	ns (min)	Valid data setup time before falling edge of SCLK.
t_5	5	ns (min)	Data hold time after SCLK falling edge.
t_6	400	ns (min)	Minimum time between the end of data byte transfers.
t_7	50	ns (min)	Minimum time between byte transfers during a serial write.
t_8	100	ns (min)	$\overline{CS}$ hold time after SCLK falling edge.
Read Timing			
t_9[3]	4	µs (min)	Minimum time between read command (i.e., a write to communication reigster) and data read.
t_{10}	50	ns (min)	Minimum time between data byte transfers during a multibyte read.
t_{11}	30	ns (min)	Data access time after SCLK rising edge following a write to the communications register.
t_{12}[4]	100	ns (max)	Bus relinquish time after falling edge of SCLK.
	10	ns (min)	
t_{13}[5]	100	ns (max)	Bus relinquish time after rising edge of $\overline{CS}$.
	10	ns (min)	

[1] Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5 ns (10% to 90%) and timed from a voltage level of 1.6 V.
[2] See Figure 3, Figure 4, and the Serial Interface section.
[3] Minimum time between read command and data read for all registers except waveform register, which is t_9 = 500 ns min.
[4] Measured with the load circuit in Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.
[5] Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

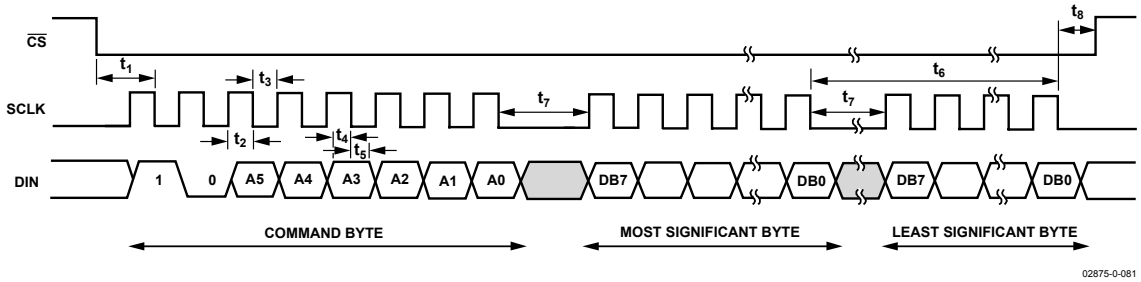

Figure 3. Serial Write Timing

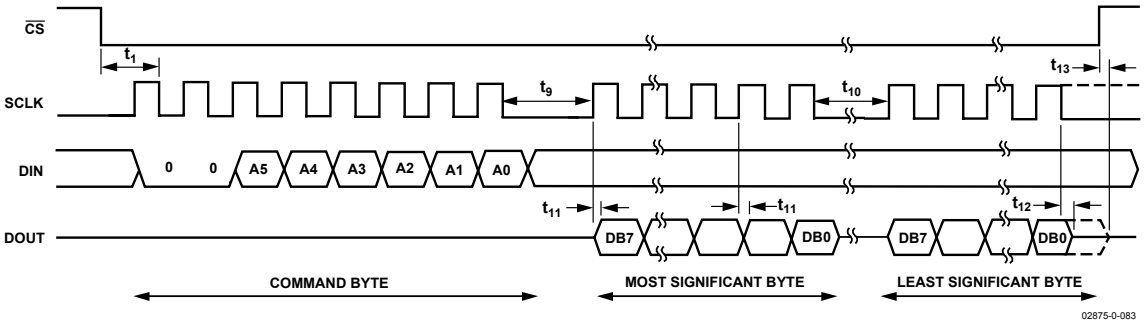

Figure 4. Serial Read Timing

ABSOLUTE MAXIMUM RATINGS

Table 3. T_A = 25°C, unless otherwise noted.

Parameter	Rating
AV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
DV_{DD} to AV_{DD}	–0.3 V to +0.3 V
Analog Input Voltage to AGND V_{1P}, V_{1N}, V_{2P}, and V_{2N}	–6 V to +6 V
Reference Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
20-Lead SSOP, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	112°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7753 is defined by the following formula:

$$Percentage\ Error = \left(\frac{Energy\ Register\ ADE7753 - True\ Energy}{True\ Energy} \right) \times 100\%$$

Phase Error between Channels

The digital integrator and the HPF (high-pass filter) in Channel 1 have non-ideal phase response. To offset this phase response and equalize the phase response between channels, two phase-correction networks are placed in Channel 1: one for the digital integrator and the other for the HPF. Each phase correction network corrects the phase response of the corresponding component and ensures a phase match between Channel 1 (current) and Channel 2 (voltage) to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range 40 Hz to 1 kHz.

Power Supply Rejection

This quantifies the ADE7753 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when an ac (175 mV rms/120 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is again expressed as a percentage of reading.

ADC Offset Error

The dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection—see the Typical Performance Characteristics. However, when HPF1 is switched on, the offset is removed from Channel 1 (current) and the power calculation is not affected by this offset. The offsets may be removed by performing an offset calibration—see the Analog Inputs section.

Gain Error

The difference between the measured ADC output code (minus the offset) and the ideal output code—see the Channel 1 ADC and Channel 2 ADC sections. It is measured for each of the input ranges on Channel 1 (0.5 V, 0.25 V, and 0.125 V). The difference is expressed as a percentage of the ideal code.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

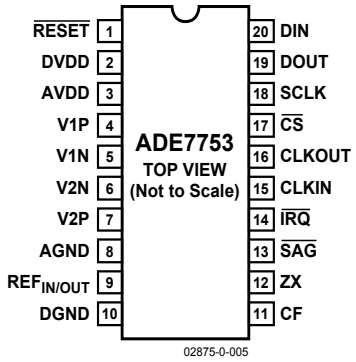

Figure 5. Pin Configuration (SSOP Package)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Reset Pin for the ADE7753. A logic low on this pin will hold the ADCs and digital circuitry (including the serial interface) in a reset condition.
2	DVDD	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7753. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
3	AVDD	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the ADE7753. The supply should be maintained at 5 V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. The typical performance graphs show the power supply rejection performance. This pin should be decoupled to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
4, 5	V1P, V1N	Analog Inputs for Channel 1. This channel is intended for use with a di/dt current transducer such as Rogowski coil or another current sensor such as shunt or current transformer (CT). These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V, ±0.25 V, and ±0.125 V, depending on the full-scale selection—see the Analog Inputs section. Channel 1 also has a PGA with gain selections of 1, 2, 4, 8, or 16. The maximum signal level at these pins with respect to AGND is ±0.5 V. Both inputs have internal ESD protection circuitry, and, in addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
6, 7	V2N, V2P	Analog Inputs for Channel 2. This channel is intended for use with the voltage transducer. These inputs are fully differential voltage inputs with a maximum differential signal level of ±0.5 V. Channel 2 also has a PGA with gain selections of 1, 2, 4, 8, or 16. The maximum signal level at these pins with respect to AGND is ±0.5 V. Both inputs have internal ESD protection circuitry, and an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
8	AGND	Analog Ground Reference. This pin provides the ground reference for the analog circuitry in the ADE7753, i.e., ADCs and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, e.g., anti-aliasing filters, current and voltage transducers, etc. To keep ground noise around the ADE7753 to a minimum, the quiet ground plane should connected to the digital ground plane at only one point. It is acceptable to place the entire device on the analog ground plane—see the Applications Information section.
9	$\text{REF}_{\text{IN/OUT}}$	Access to the On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.4 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor.
10	DGND	Digital Ground Reference. This pin provides the ground reference for the digital circuitry in the ADE7753, i.e., multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the ADE7753 are small, it is acceptable to connect this pin to the analog ground plane of the system—see the Applications Information section. However, high bus capacitance on the DOUT pin may result in noisy digital current, which could affect performance.
11	CF	Calibration Frequency Logic Output. The CF logic output gives active power information. This output is intended to be used for operational and calibration purposes. The full-scale output frequency can be adjusted by writing to the CFDEN and CFNUM registers—see the Energy-to-Frequency Conversion section.

Pin No.	Mnemonic	Description
12	ZX	Voltage Waveform (Channel 2) Zero-Crossing Output. This output toggles logic high and logic low at the zero crossing of the differential signal on Channel 2—see the Zero Crosssing Detection section.
13	$\overline{\text{SAG}}$	This open-drain logic output goes active low when either no zero crossings are detected or a low voltage threshold (Channel 2) is crossed for a specified duration—see the Line Voltage Sag Detection section.
14	$\overline{\text{IRQ}}$	Interrupt Request Output. This is an active low open-drain logic output. Maskable interrupts include active energy register rollover, active energy register at half level, and arrivals of new waveform samples—see the ADE7753 Interrupts section.
15	CLKIN	Master Clock for ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7753. The clock frequency for specified operation is 3.579545 MHz. Ceramic load capacitors of between 22 pF and 33 pF should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for load capacitance requirements.
16	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the ADE7753. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
17	$\overline{\text{CS}}$	Chip Select. Part of the 4-wire SPI serial interface. This active low logic input allows the ADE7753 to share the serial bus with several other devices—see the ADE7753 Serial Interface section.
18	SCLK	Serial Clock Input for the Synchronous Serial Interface. All serial data transfers are synchronized to this clock—see the ADE7753 Serial Interface section. The SCLK has a Schmitt-trigger input for use with a clock source that has a slow edge transition time, e.g., opto-isolator outputs.
19	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state unless it is driving data onto the serial data bus—see the ADE7753 Serial Interface section.
20	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK—see the ADE7753 Serial Interface section.

TYPICAL PERFORMANCE CHARACTERISTICS

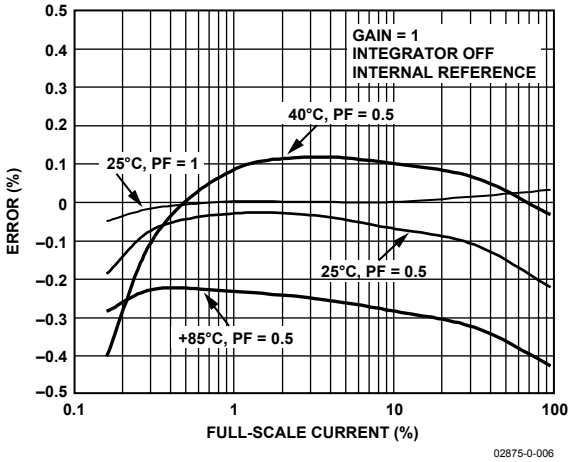

Figure 6. Active Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference and Integrator Off

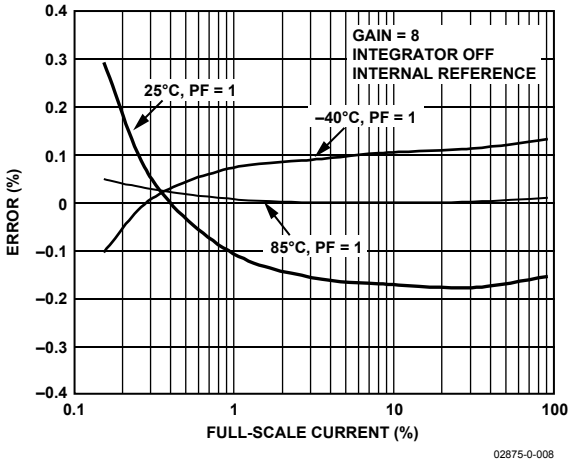

Figure 7. Active Energy as a Percentage of Reading (Gain = 8) over Temperature with Internal Reference and Integrator Off

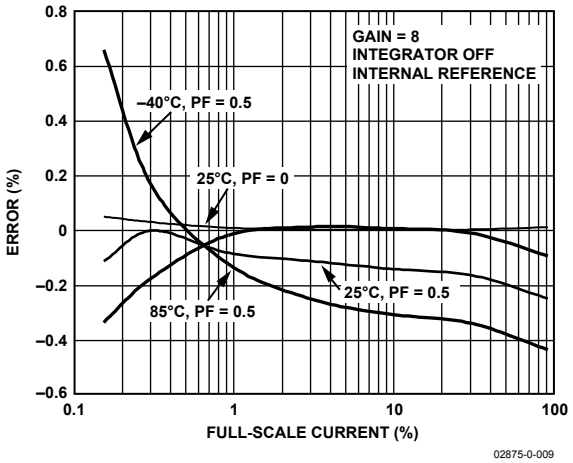

Figure 8. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator Off

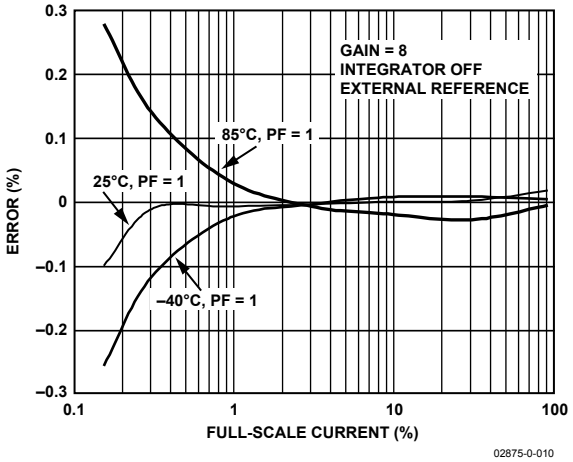

Figure 9. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with External Reference and Integrator Off

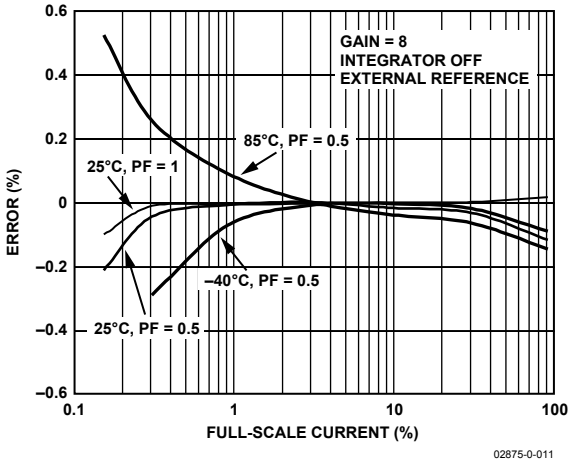

Figure 10. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with External Reference and Integrator Off

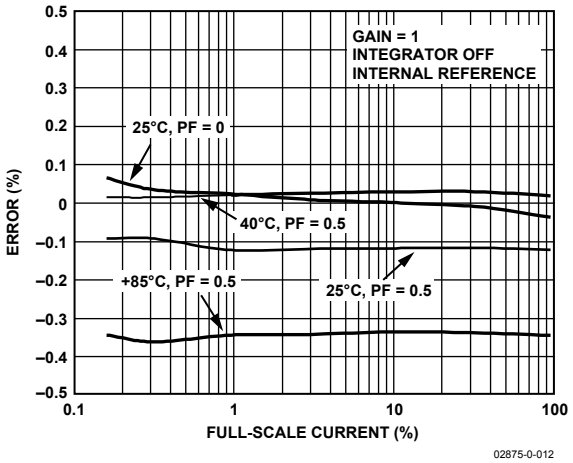

Figure 11. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference and Integrator Off

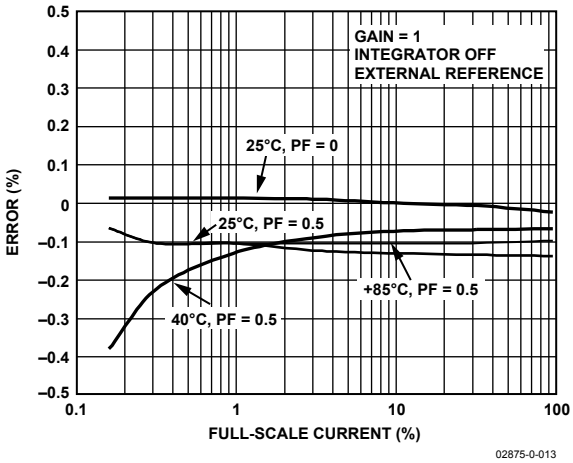

Figure 12. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Temperature with External Reference and Integrator Off

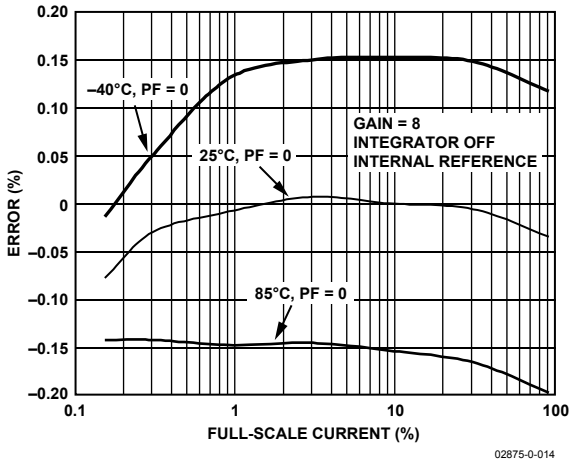

Figure 13. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator Off

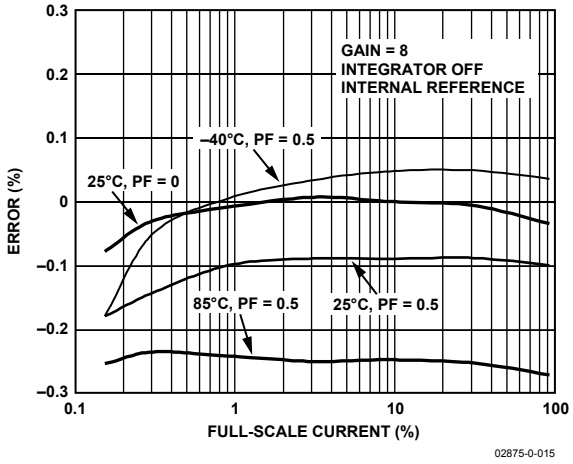

Figure 14. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator Off

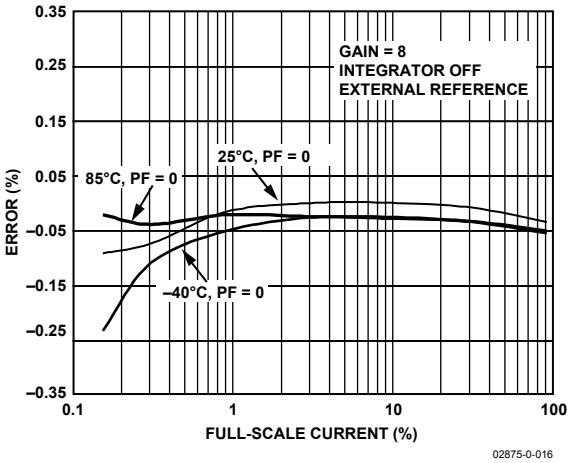

Figure 15. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Temperature with External Reference and Integrator Off

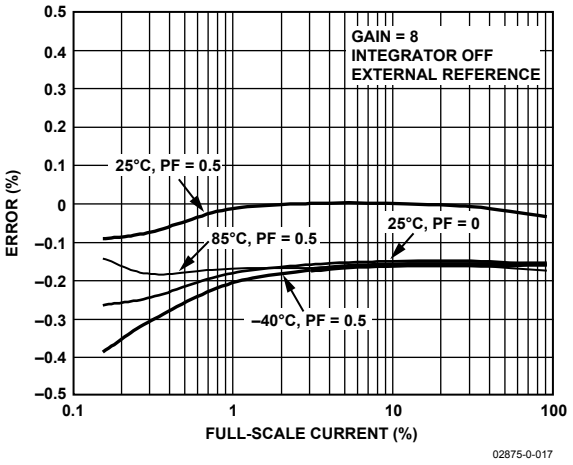

Figure 16. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with External Reference and Integrator Off

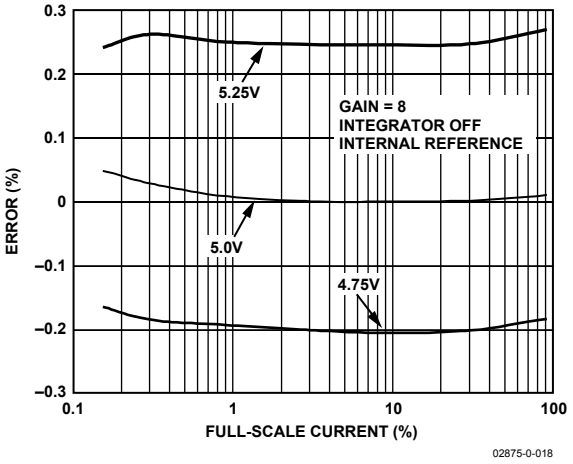

Figure 17. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Supply with Internal Reference and Integrator Off

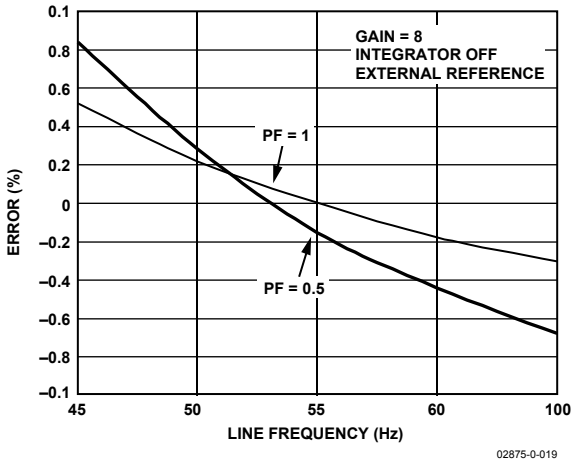

Figure 18. Active Energy Error as a Percentage of Reading (Gain = 8) over Frequency with External Reference and Integrator Off

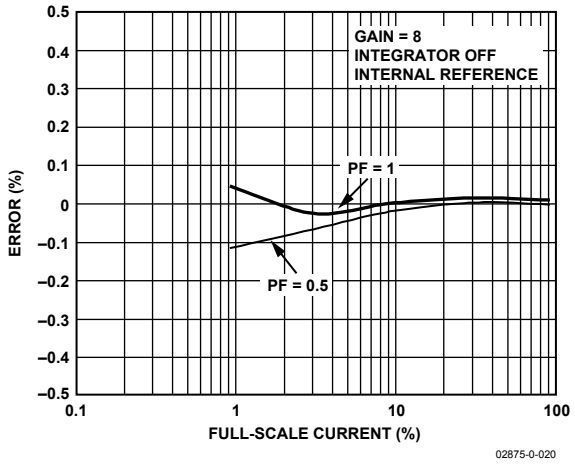

Figure 19. IRMS Error as a Percentage of Reading (Gain = 8) with Internal Reference and Integrator Off

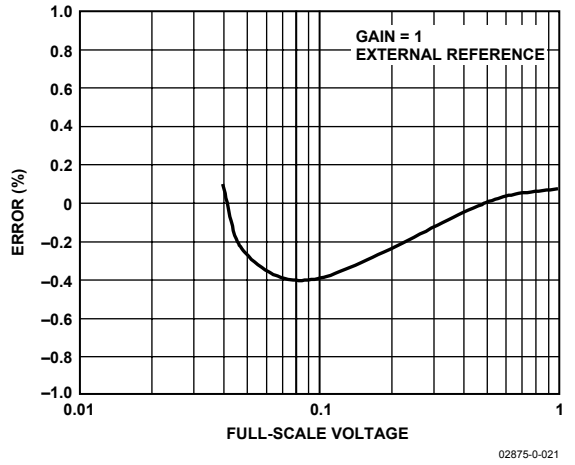

Figure 20. VRMS Error as a Percentage of Reading (Gain = 1) with External Reference

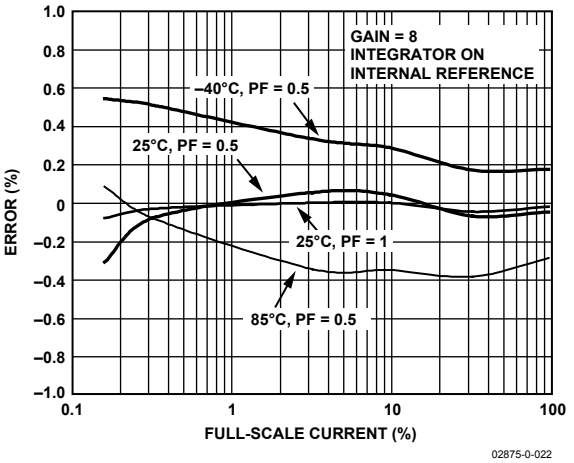

Figure 21. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator On

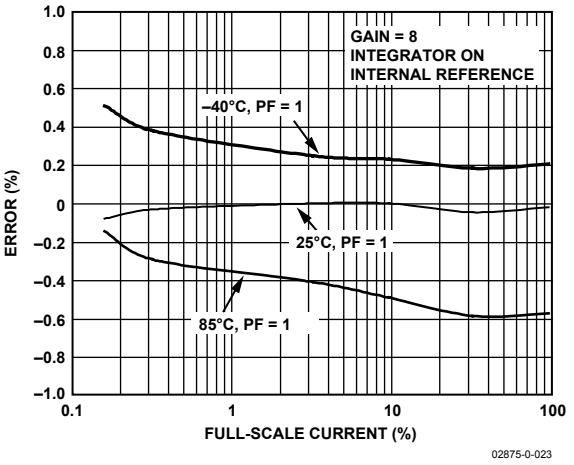

Figure 22. Active Energy Error as a Percentage of Reading (Gain = 8) over Temperature with Internal Reference and Integrator On

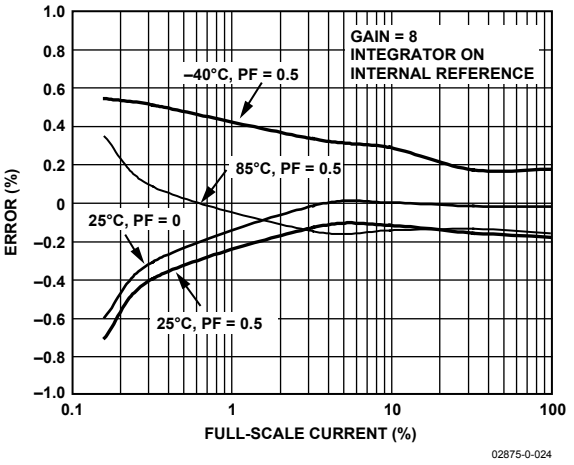

Figure 23. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator On

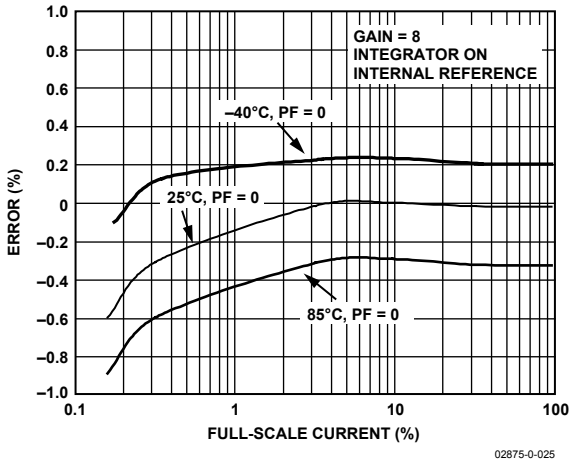

Figure 24. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator On

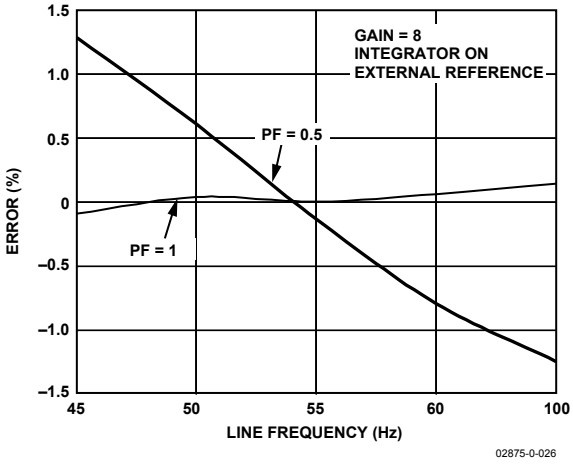

Figure 25. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with External Reference and Integrator On

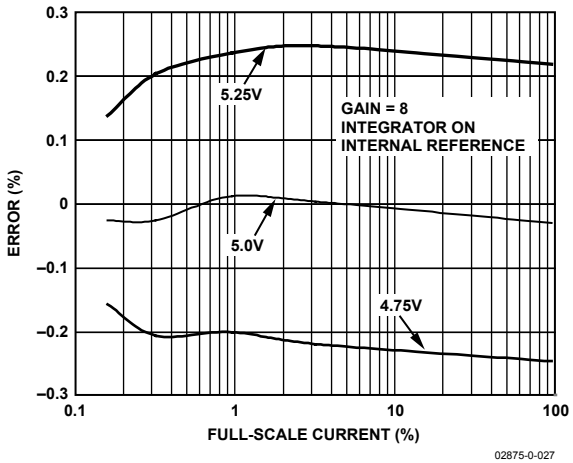

Figure 26. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Supply with Internal Reference and Integrator On

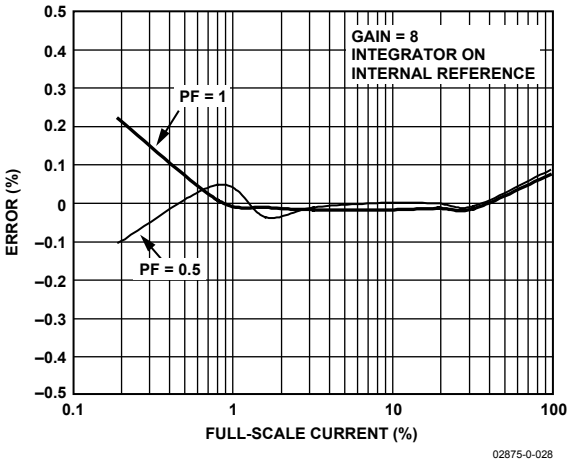

Figure 27. IRMS Error as a Percentage of Reading (Gain = 8) with Internal Reference and Integrator On

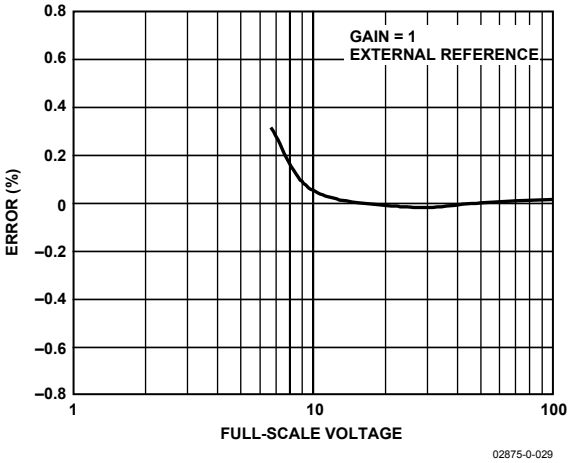

Figure 28.VRMS Error as a Percentage of Reading (Gain = 1) with External Reference

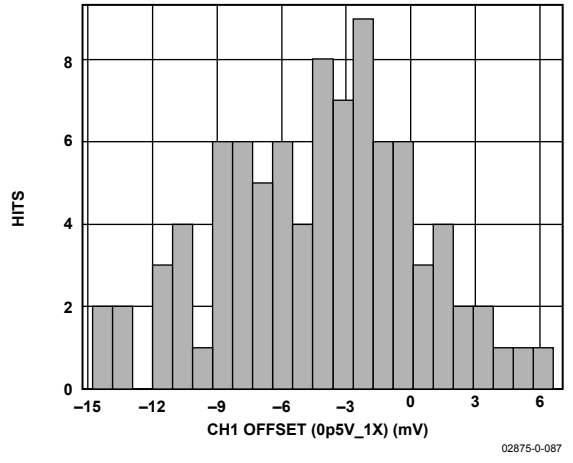

Figure 29. Channel 1 Offset (Gain = 1)

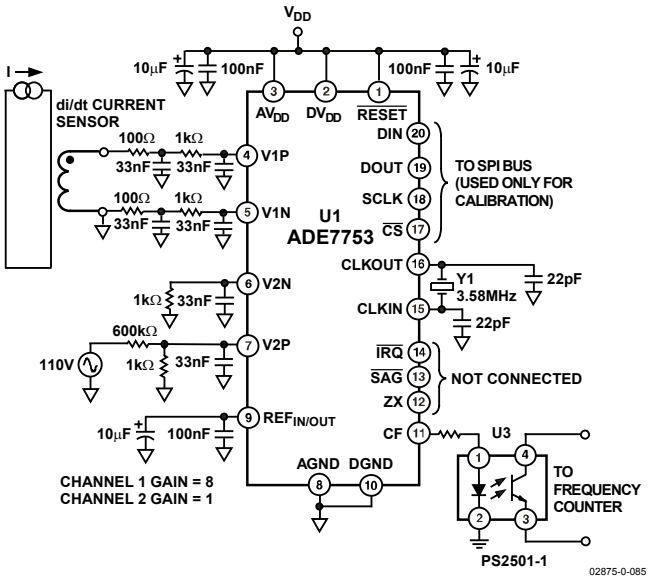

Figure 30. Test Circuit for Performance Curves with Integrator On

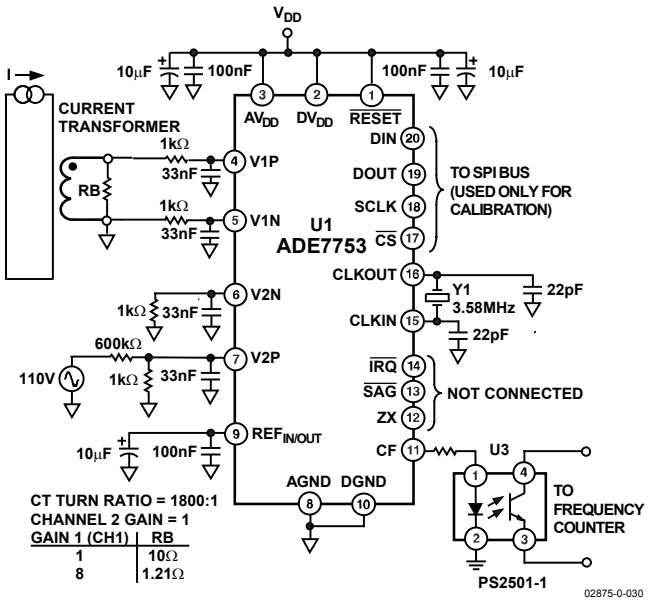

Figure 31. Test Circuit for Performance Curves with Integrator Off

THEORY OF OPERATION

ANALOG INPUTS

The ADE7753 has two fully differential voltage input channels. The maximum differential input voltage for input pairs V1P/V1N and V2P/V2N are ±0.5 V. In addition, the maximum signal level on analog inputs for V1P/V1N and V2P/ V2N are ±0.5 V with respect to AGND.

Each analog input channel has a PGA (programmable gain amplifier) with possible gain selections of 1, 2, 4, 8, and 16. The gain selections are made by writing to the gain register—see Figure 33. Bits 0 to 2 select the gain for the PGA in Channel 1, and the gain selection for the PGA in Channel 2 is made via Bits 5 to 7. Figure 32 shows how a gain selection for Channel 1 is made using the gain register.

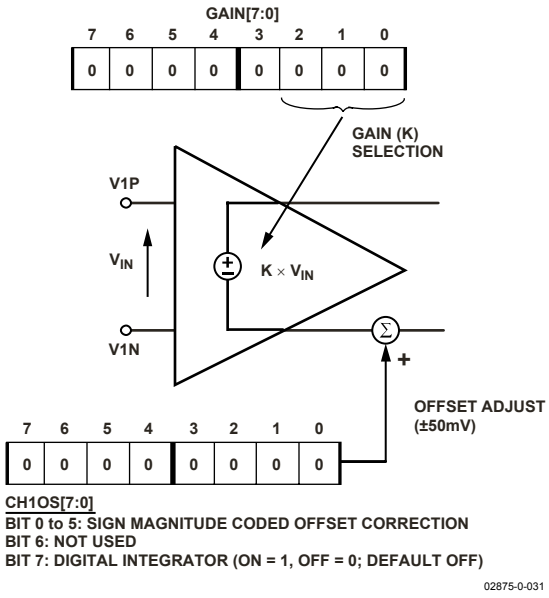

Figure 32. PGA in Channel 1

In addition to the PGA, Channel 1 also has a full-scale input range selection for the ADC. The ADC analog input range selection is also made using the gain register—see Figure 33. As mentioned previously, the maximum differential input voltage is 0.5 V. However, by using Bits 3 and 4 in the gain register, the maximum ADC input voltage can be set to 0.5 V, 0.25 V, or 0.125 V. This is achieved by adjusting the ADC reference—see the ADE7753 Reference Circuit section. Table 5 summarizes the maximum differential input signal level on Channel 1 for the various ADC range and gain selections.

Table 5. Maximum Input Signal Levels for Channel 1

Max Signal	ADC Input Range Selection		
Channel 1	**0.5 V**	**0.25 V**	**0.125 V**
0.5 V	Gain = 1	–	–
0.25 V	Gain = 2	Gain = 1	–
0.125 V	Gain = 4	Gain = 2	Gain = 1
0.0625 V	Gain = 8	Gain = 4	Gain = 2
0.0313 V	Gain = 16	Gain = 8	Gain = 4
0.0156 V	–	Gain = 16	Gain = 8
0.00781 V	–	–	Gain = 16

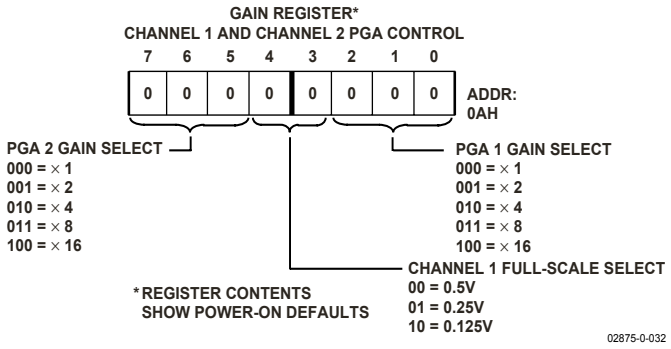

Figure 33. ADE7753 Analog Gain Register

It is also possible to adjust offset errors on Channel 1 and Channel 2 by writing to the offset correction registers (CH1OS and CH2OS, respectively). These registers allow channel offsets in the range ±20 mV to ±50 mV (depending on the gain setting) to be removed. Note that it is not necessary to perform an offset correction in an energy measurement application if HPF in Channel 1 is switched on. Figure 34 shows the effect of offsets on the real power calculation. As seen from Figure 34, an offset on Channel 1 and Channel 2 will contribute a dc component after multiplication. Since this dc component is extracted by LPF2 to generate the active (real) power information, the offsets will have contributed an error to the active power calculation. This problem is easily avoided by enabling HPF in Channel 1. By removing the offset from at least one channel, no error component is generated at dc by the multiplication. Error terms at cos(ωt) are removed by LPF2 and by integration of the active power signal in the active energy register (AENERGY[23:0])—see the Energy Calculation section.

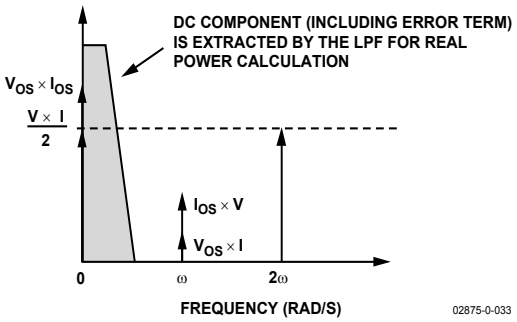

Figure 34. Effect of Channel Offsets on the Real Power Calculation

The contents of the offset correction registers are 6-bit, sign and magnitude coded. The weight of the LSB depends on the gain setting, i.e., 1, 2, 4, 8, or 16. Table 6 shows the correctable offset span for each of the gain settings and the LSB weight (mV) for the offset correction registers. The maximum value that can be written to the offset correction registers is ±31d—see Figure 35. Figure 35 shows the relationship between the offset correction register contents and the offset (mV) on the analog inputs for a gain setting of 1. In order to perform an offset adjustment, the analog inputs should be first connected to AGND, and there should be no signal on either Channel 1 or Channel 2. A read from Channel 1 or Channel 2 using the waveform register will indicate the offset in the channel. This offset can be canceled by writing an equal and opposite offset value to the Channel 1 offset register, or an equal value to the Channel 2 offset register. The offset correction can be confirmed by performing another read. Note when adjusting the offset of Channel 1, one should disable the digital integrator and the HPF.

Table 6. Offset Correction Range—Channels 1 and 2

Gain	Correctable Span	LSB Size
1	±50 mV	1.61 mV/LSB
2	±37 mV	1.19 mV/LSB
4	±30 mV	0.97 mV/LSB
8	±26 mV	0.84 mV/LSB
16	±24 mV	0.77 mV/LSB

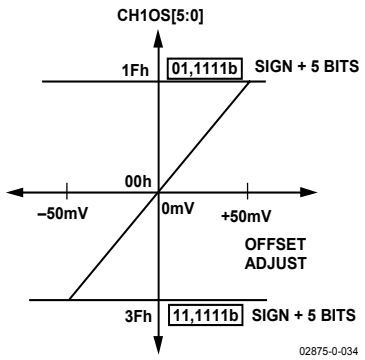

Figure 35. Channel 1 Offset Correction Range (Gain = 1)

The current and voltage rms offsets can be adjusted with the IRMSOS and VRMSOS registers—see Channel 1 RMS Offset Compensation and Channel 2 RMS Offset Compensation sections.

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR

A di/dt sensor detects changes in magnetic field caused by ac current. Figure 36 shows the principle of a di/dt current sensor.

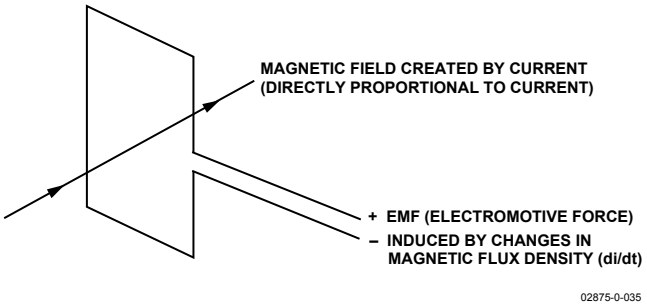

Figure 36. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal, which is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current carrying conductor and the di/dt sensor. The current signal needs to be recovered from the di/dt signal before it can be used. An integrator is therefore necessary to restore the signal to its original form. The ADE7753 has a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator on Channel 1 is switched off by default when the ADE7753 is powered up. Setting the MSB of CH1OS register will turn on the integrator. Figure 37 to Figure 40 show the magnitude and phase response of the digital integrator.

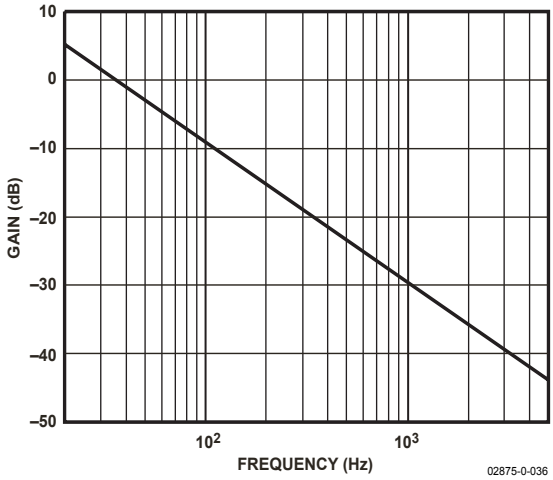

Figure 37. Combined Gain Response of the Digital Integrator and Phase Compensator

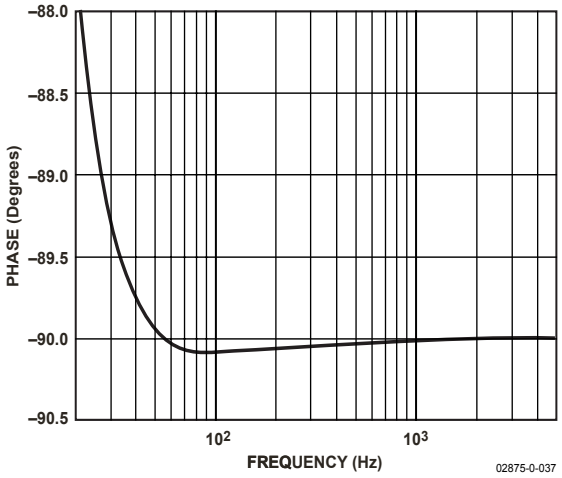

Figure 38. Combined Phase Response of the Digital Integrator and Phase Compensator

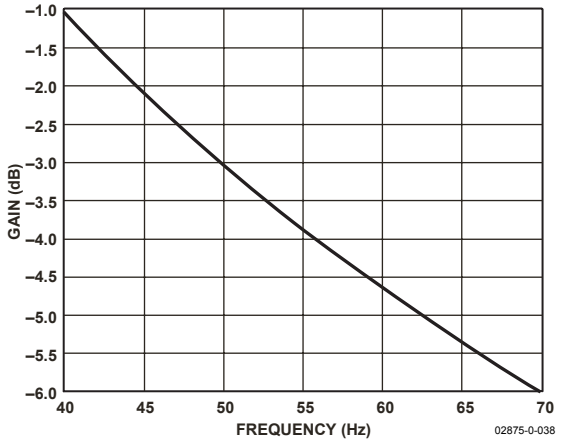

Figure 39. Combined Gain Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

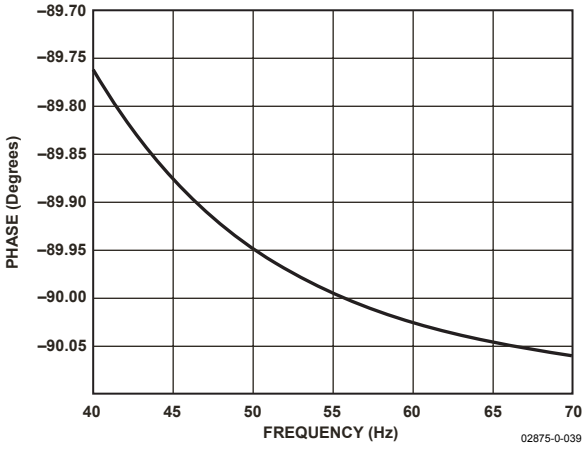

Figure 40. Combined Phase Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

Note that the integrator has a –20 dB/dec attenuation and approximately –90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. The di/dt sensor has a 20 dB/dec gain associated with it. It also generates significant high frequency noise, therefore a more effective antialiasing filter is needed to avoid noise due to aliasing—see the Antialias Filter section.

When the digital integrator is switched off, the ADE7753 can be used directly with a conventional current sensor such as current transformer (CT) or with a low resistance current shunt.

ZERO-CROSSING DETECTION

The ADE7753 has a zero-crossing detection circuit on Channel 2. This zero crossing is used to produce an external zero-crossing signal (ZX), and it is also used in the calibration mode—see the Energy Calibration section. The zero-crossing signal is also used to initiate a temperature measurement on the ADE7753—see the Temperature Measurement section.

Figure 41 shows how the zero-crossing signal is generated from the output of LPF1.

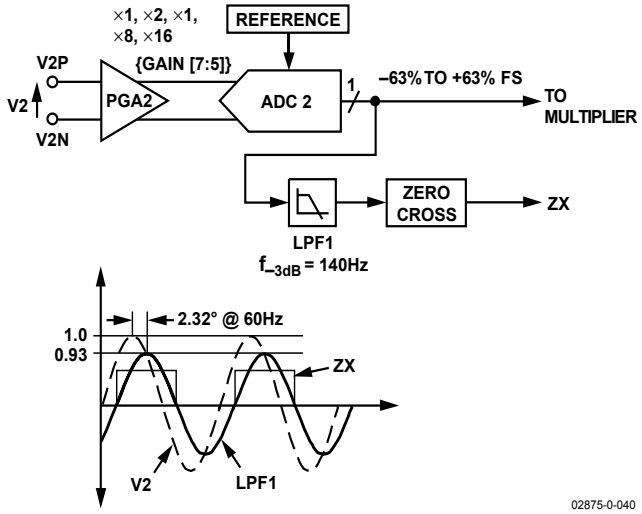

Figure 41. Zero-Crossing Detection on Channel 2

The ZX signal will go logic high on a positive going zero crossing and logic low on a negative going zero crossing on Channel 2. The zero-crossing signal ZX is generated from the output of LPF1. LPF1 has a single pole at 140 Hz (at CLKIN = 3.579545 MHz). As a result, there will be a phase lag between the analog input signal V2 and the output of LPF1. The phase response of this filter is shown in the Channel 2 Sampling section. The phase lag response of LPF1 results in a time delay of approximately 1.14 ms (@ 60 Hz) between the zero crossing on the analog inputs of Channel 2 and the rising or falling edge of ZX.

The zero-crossing detection also drives the ZX flag in the interrupt status register. An active low in the IRQ output will also appear if the corresponding bit in the interrupt enable register is set to Logic 1.

The flag in the interrupt status register as well as the IRQ output are reset to their default values when the interrupt status register with reset (RSTSTATUS) is read.

Zero-Crossing Timeout

The zero-crossing detection also has an associated timeout register, ZXTOUT. This unsigned, 12-bit register is decremented (1 LSB) every 128/CLKIN seconds. The register is reset to its user programmed full-scale value every time a zero crossing on Channel 2 is detected. The default power on value in this register is FFFh. If the internal register decrements to 0 before a zero crossing is detected and the DISSAG bit in the mode register is Logic 0, the $\overline{\text{SAG}}$ pin will go active low. The absence of a zero crossing is also indicated on the $\overline{\text{IRQ}}$ pin if the ZXTO enable bit in the interrupt enable register is set to Logic 1. Irrespective of the enable bit setting, the ZXTO flag in the interrupt status register is always set when the internal ZXTOUT register is decremented to 0—see the ADE7753 Interrupts section.

The ZXOUT register can be written/read by the user and has an address of 1Dh—see the Serial Interface section. The resolution of the register is 128/CLKIN seconds per LSB. Thus the maximum delay for an interrupt is 0.15 second (128/CLKIN × 2^{12}).

Figure 42 shows the mechanism of the zero-crossing timeout detection when the line voltage stays at a fixed dc level for more than CLKIN/128 × ZXTOUT seconds.

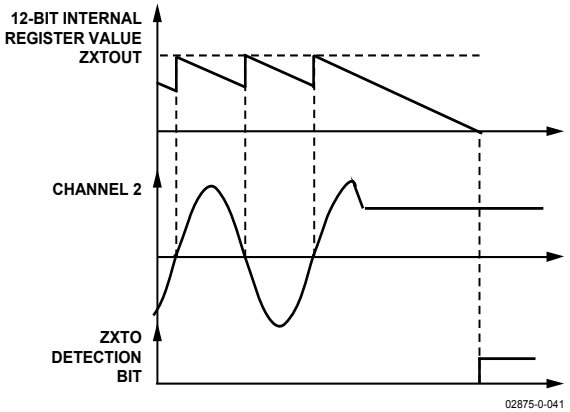

Figure 42. Zero-Crossing Timeout Detection

PERIOD MEASUREMENT

The ADE7753 also provides the period measurement of the line. The period register is an unsigned 15-bit register and is updated every period.

The resolution of this register is 2.2 ms/LSB when CLKIN = 3.579545 MHz, which represents 0.013% when the line frequency is 60 Hz. When the line frequency is 60 Hz, the value of the period register is approximately 7576d. The length of the register enables the measurement of line frequencies as low as 13.9 Hz.

The period register is stable at ±1 LSB when the line is established and the measurement does not change. A settling time of 1.8 seconds is associated with this filter before the measurement is stable.

POWER SUPPLY MONITOR

The ADE7753 also contains an on-chip power supply monitor. The analog supply (AV_{DD}) is continuously monitored by the ADE7753. If the supply is less than 4 V ± 5%, then the ADE7753 will go into an inactive state, i.e., no energy will be accumulated when the supply voltage is below 4 V. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which give a high degree of immunity to false triggering due to noisy supplies.

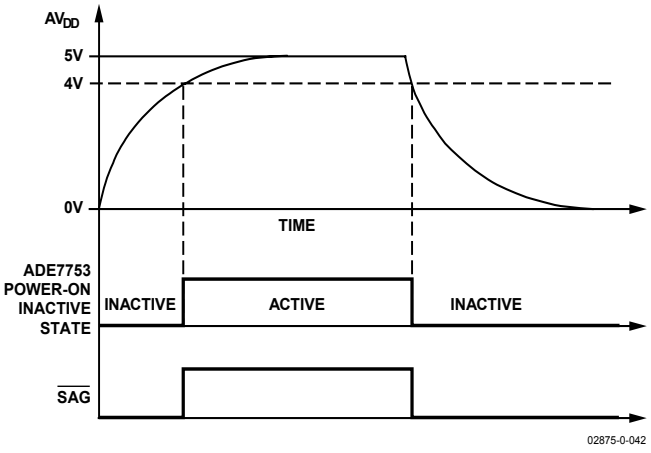

Figure 43. On-Chip Power Supply Monitor

As seen from Figure 43, the trigger level is nominally set at 4 V. The tolerance on this trigger level is about ±5%. The $\overline{\text{SAG}}$ pin can also be used as a power supply monitor input to the MCU. The $\overline{\text{SAG}}$ pin will go logic low when the ADE7753 is in its inactive state. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed 5 V ±5%, as specified for normal operation.

LINE VOLTAGE SAG DETECTION

In addition to the detection of the loss of the line voltage signal (zero crossing), the ADE7753 can also be programmed to detect when the absolute value of the line voltage drops below a certain peak value for a number of line cycles. This condition is illustrated in Figure 44.

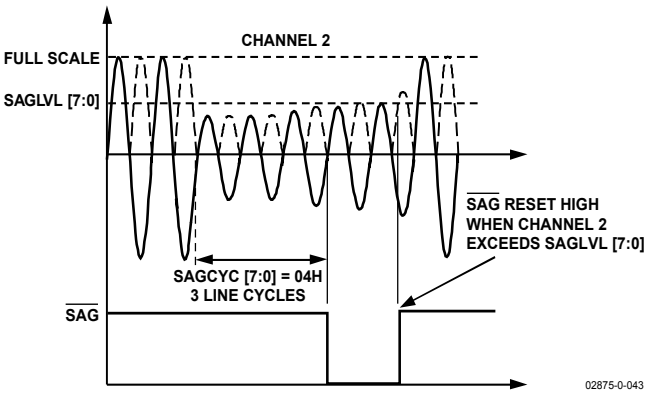

Figure 44. ADE7753 Sag Detection

Figure 44 shows the line voltage falling below a threshold that is set in the sag level register (SAGLVL[7:0]) for three line cycles. The quantities 0 and 1 are not valid for the SAGCYC register, and the contents represent one more than the desired number of full line cycles. For example, when the sag cycle (SAGCYC[7:0]) contains 04h, the $\overline{\text{SAG}}$ pin will go active low at the end of the third line cycle for which the line voltage (Channel 2 signal) falls below the threshold, if the DISSAG bit in the mode register is Logic 0. As is the case when zero crossings are no longer detected, the sag event is also recorded by setting the SAG flag in the interrupt status register. If the SAG enable bit is set to Logic 1, the IRQ logic output will go active low—see the ADE7753 Interrupts section. The $\overline{\text{SAG}}$ pin will go logic high again when the absolute value of the signal on Channel 2 exceeds the sag level set in the sag level register. This is shown in Figure 44 when the $\overline{\text{SAG}}$ pin goes high again during the fifth line cycle from the time when the signal on Channel 2 first dropped below the threshold level.

Sag Level Set

The contents of the sag level register (1 byte) are compared to the absolute value of the most significant byte output from LPF1 after it is shifted left by one bit, thus, for example, the nominal maximum code from LPF1 with a full-scale signal on Channel 2 is 2518h—see the Channel 2 Sampling section. Shifting one bit left will give 4A30h. Therefore writing 4Ah to the SAG level register will put the sag detection level at full scale. Writing 00h or 01h will put the sag detection level at 0. The SAG level register is compared to the most significant byte of a waveform sample after the shift left and detection is made when the contents of the sag level register are greater.

PEAK DETECTION

The ADE7753 can also be programmed to detect when the absolute value of the voltage or current channel exceeds a specified peak value. Figure 45 illustrates the behavior of the peak detection for the voltage channel.

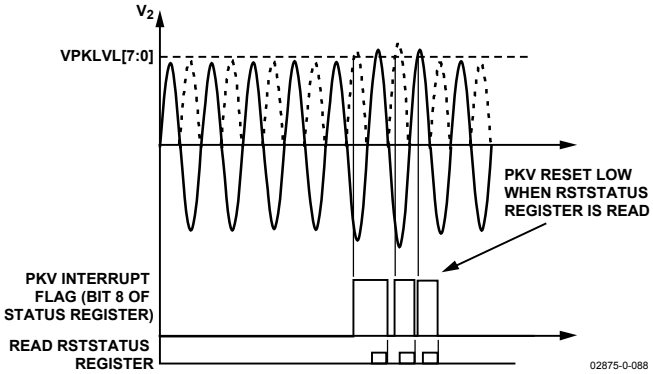

Figure 45. ADE7753 Peak Level Detection

Both Channel 1 and Channel 2 are monitored at the same time.

Figure 45 shows a line voltage exceeding a threshold that is set in the voltage peak register (VPKLVL[7:0]). The voltage peak event is recorded by setting the PKV flag in the interrupt status register. If the PKV enable bit is set to Logic 1 in the interrupt mask register, the IRQ logic output will go active low. Similarly, the current peak event is recorded by setting the PKI flag in the interrupt status register—see the ADE7753 Interrupts section.

Peak Level Set

The contents of the VPKLVL and IPKLVL registers are respectively compared to the absolute value of Channel 1 and Channel 2 after they are multiplied by 2.Thus, for example, the nominal maximum code from the Channel 1 ADC with a full-scale signal is 2851ECh—see the Channel 1 Sampling section. Multiplying by 2 will give 50A3D8h. Therefore, writing 50h to the IPKLVL register, for example, will put the Channel 1 peak detection level at full scale and set the current peak detection to its least sensitive value. Writing 00h will put the Channel 1 detection level at 0. The detection is done by comparing the contents of the IPKLVL register to the incoming Channel 1 sample. The $\overline{\text{IRQ}}$ pin indicates that the peak level is exceeded if the PKI or PKV bits are set in the interrupt enable register (IRQEN[15:0]) at Address 0Ah.

Peak Level Record

The ADE7753 records the maximum absolute value reached by Channel 1 and Channel 2 in two different registers—IPEAK and VPEAK, respectively. VPEAK and IPEAK are 24-bit unsigned registers. These registers are updated each time the absolute value of the waveform sample from the corresponding channel is above the value stored in the VPEAK or IPEAK register. The contents of the VPEAK register corresponds to 2 times the maximum absolute value observed on the Channel 2

input. The contents of IPEAK represents the maximum absolute value observed on the Channel 1 input. Reading the RSTVPEAK and RSTIPEAK registers will clear their respective contents after the read operation.

ADE7753 INTERRUPTS

ADE7753 interrupts are managed through the interrupt status register (STATUS[15:0]) and the interrupt enable register (IRQEN[15:0]). When an interrupt event occurs in the ADE7753, the corresponding flag in the status register is set to Logic 1—see the Interrupt Status Register section. If the enable bit for this interrupt in the interrupt enable register is Logic 1, then the IRQ logic output goes active low. The flag bits in the status register are set irrespective of the state of the enable bits.

To determine the source of the interrupt, the system master (MCU) should perform a read from the status register with reset (RSTSTATUS[15:0]). This is achieved by carrying out a read from Address 0Ch. The IRQ output will go logic high on completion of the interrupt status register read command—see the Interrupt Timing section. When carrying out a read with reset, the ADE7753 is designed to ensure that no interrupt events are missed. If an interrupt event occurs just as the status register is being read, the event will not be lost and the IRQ logic output is guaranteed to go high for the duration of the interrupt status register data transfer before going logic low again to indicate the pending interrupt. See the next section for a more detailed description.

Using the ADE7753 Interrupts with an MCU

Figure 47 shows a timing diagram that shows a suggested implementation of ADE7753 interrupt management using an MCU. At time t_1, the IRQ line will go active low indicating that one or more interrupt events have occurred in the ADE7753. The IRQ logic output should be tied to a negative edge-triggered external interrupt on the MCU. On detection of the negative edge, the MCU should be configured to start executing its interrupt service routine (ISR). On entering the ISR, all interrupts should be disabled by using the global interrupt enable bit. At this point, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR. When the MCU interrupt flag is cleared, a read from the status register with reset is carried out. This will cause the IRQ line to be reset logic high (t_2)—see the Interrupt Timing section. The status register contents are used to determine the source of the interrupt(s) and therefore the appropriate action to be taken. If a subsequent interrupt event occurs during the ISR, that event will be recorded by the MCU external interrupt flag being set again (t_3). On returning from the ISR, the global interrupt mask will be cleared (same instruction cycle) and the external interrupt flag will cause the MCU to jump to its ISR once a gain. This will ensure that the MCU does not miss any external interrupts.

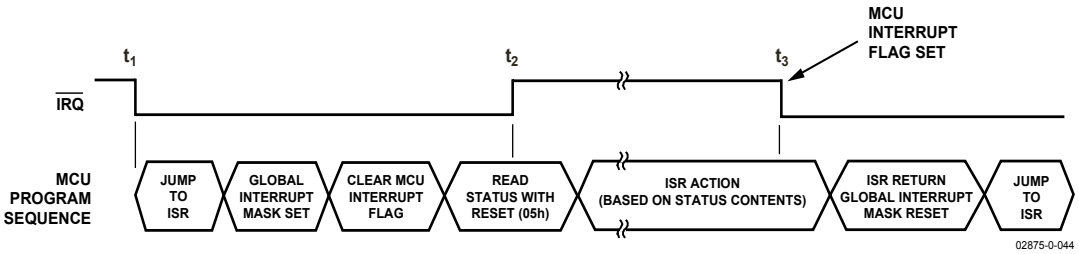

Figure 46. ADE7753 Interrupt Management

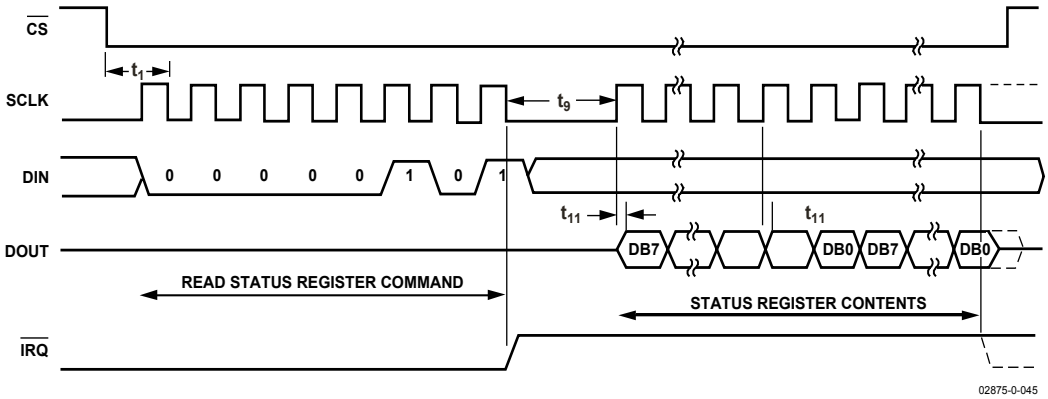

Figure 47. ADE7753 Interrupt Timing

Interrupt Timing

The ADE7753 Serial Interface section should be reviewed first before reviewing the interrupt timing. As previously described, when the IRQ output goes low, the MCU ISR must read the interrupt status register to determine the source of the interrupt. When reading the status register contents, the IRQ output is set high on the last falling edge of SCLK of the first byte transfer (read interrupt status register command). The IRQ output is held high until the last bit of the next 15-bit transfer is shifted out (interrupt status register contents)—see Figure 46. If an interrupt is pending at this time, the IRQ output will go low again. If no interrupt is pending, the IRQ output will stay high.

TEMPERATURE MEASUREMENT

The ADE7753 also includes an on-chip temperature sensor. A temperature measurement can be made by setting Bit 5 in the mode register. When Bit 5 is set logic high in the mode register, the ADE7753 will initiate a temperature measurement on the next zero crossing. When the zero crossing on Channel 2 is detected, the voltage output from the temperature sensing circuit is connected to ADC1 (Channel 1) for digitizing. The resulting code is processed and placed in the temperature register (TEMP[7:0]) approximately 26 µs later (24 CLKIN cycles). If enabled in the interrupt enable register (Bit 5), the IRQ output will go active low when the temperature conversion is finished.

The contents of the temperature register are signed (twos complement) with a resolution of approximately 1.5 LSB/°C. The temperature register will produce a code of 00h when the ambient temperature is approximately 70°C. The temperature measurement is uncalibrated in the ADE7753 and has an offset tolerance that could be as high as ±20°C.

ADE7753 ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital conversion in the ADE7753 is carried out using two second order Σ-Δ ADCs. For simplicity, the block diagram in Figure 48 shows a first order Σ-Δ ADC. The converter is made up of two parts: the Σ-Δ modulator and the digital low-pass filter.

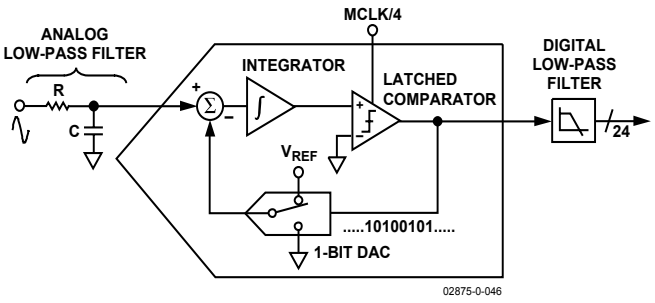

Figure 48. First Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7753, the sampling clock is equal to CLKIN/4. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) will approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged will a meaningful result be obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency), which is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7753 is CLKIN/4 (894 kHz) and the band of interest is 40 Hz to 2 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered—see Figure 49. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass type response for the quantization noise. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 49.

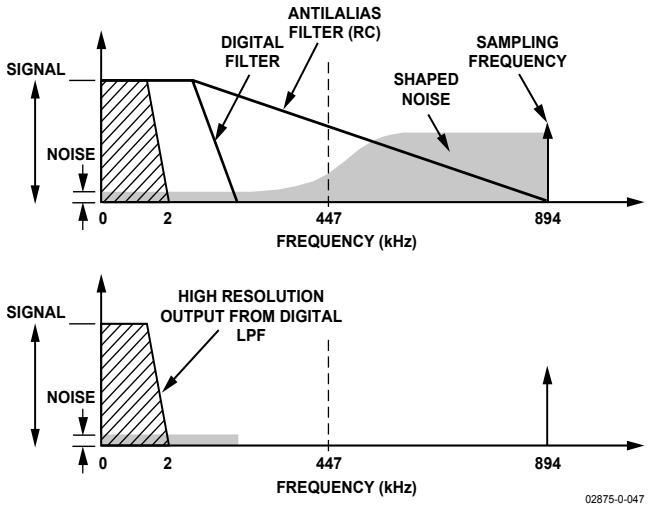

Figure 49. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialias Filter

Figure 48 also shows an analog low-pass filter (RC) on the input to the modulator. This filter is present to prevent aliasing. Aliasing is an artifact of all sampled systems. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC will appear in the sampled signal at a frequency below half the sampling rate. Figure 50 illustrates the effect. Frequency components (arrows shown in black) above half the sampling frequency (also know as the Nyquist frequency, i.e., 447 kHz) get imaged or folded back down below 447 kHz. This will happen with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, i.e., 894 kHz, will move into the band of interest for metering, i.e., 40 Hz to 2 kHz. This allows the use of a very simple LPF (low-pass filter) to attenuate high frequency (near 900 kHz) noise, and prevents distortion in the band of interest. For conventional current sensors, a simple RC filter (single-pole LPF) with a corner frequency of 10 kHz will produce an attenuation of approximately 40 dB at 894 kHz—see Figure 50. The 20 dB per decade attenuation is usually sufficient to eliminate the effects of aliasing for conventional current sensors. However, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This will neutralize the –20 dB per decade attenuation produced by one simple LPF. Therefore, when using a di/dt sensor, care should be taken to offset the 20 dB per decade gain. One simple approach is to cascade two RC filters to produce the –40 dB per decade attenuation needed.

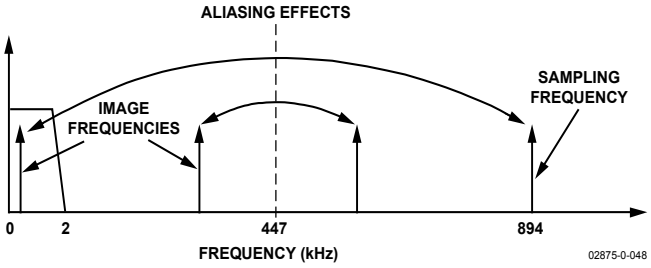

Figure 50. ADC and Signal Processing in Channel 1 Outline Dimensions

ADC Transfer Function

The following expression relates the output of the LPF in the Σ-Δ ADC to the analog input signal level. Both ADCs in the ADE7753 are designed to produce the same output code for the same input signal level.

$$Code\ (ADC) = 3.0492 \times \frac{V_{IN}}{V_{OUT}} \times 262{,}144 \quad (1)$$

Therefore with a full-scale signal on the input of 0.5 V and an internal reference of 2.42 V, the ADC output code is nominally 165,151 or 2851Fh. The maximum code from the ADC is ±262,144; this is equivalent to an input signal level of ±0.794 V. However, for specified performance, it is recommended that the full-scale input signal level of 0.5 V not be exceeded.

ADE7753 Reference Circuit

Figure 51 shows a simplified version of the reference output circuitry. The nominal reference voltage at the $REF_{IN/OUT}$ pin is 2.42 V. This is the reference voltage used for the ADCs in the ADE7753. However, Channel 1 has three input range selections that are selected by dividing down the reference value used for the ADC in Channel 1. The reference value used for Channel 1 is divided down to ½ and ¼ of the nominal value by using an internal resistor divider, as shown in Figure 51.

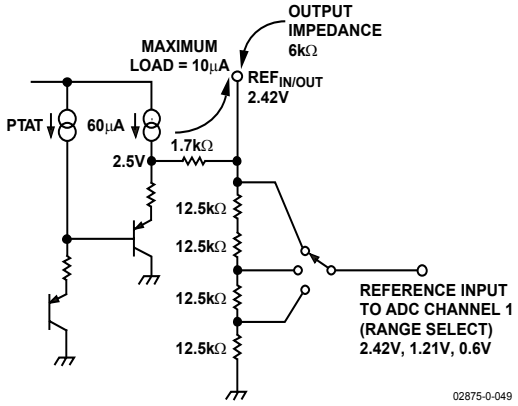

Figure 51. ADE7753 Reference Circuit Output

The $REF_{IN/OUT}$ pin can be overdriven by an external source, e.g., an external 2.5 V reference. Note that the nominal reference value supplied to the ADCs is now 2.5 V, not 2.42 V, which has the effect of increasing the nominal analog input signal range by 2.5/2.42 × 100% = 3% or from 0.5 V to 0.5165 V.

The voltage of ADE7753 reference drifts slightly with temperature—see the ADE7753 Specifications for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Since the reference is used for the ADCs in both Channels 1 and 2, any x% drift in the reference will result in 2x% deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and it is typically much smaller than the drift of other components on a meter. However, if guaranteed temperature performance is needed, one needs to use an external voltage reference. Alternatively, the meter can be calibrated at multiple temperatures. Real-time compensation can be achieved easily by usingthe on-chip temperature sensor.

CHANNEL 1 ADC

Figure 52 shows the ADC and signal processing chain for Channel 1. In waveform sampling mode, the ADC outputs a signed twos complement 24-bit data-word at a maximum of 27.9 kSPS (CLKIN/128). With the specified full-scale analog input signal of 0.5 V (or 0.25 V or 0.125 V—see the Analog Inputs section) the ADC will produce an output code that is approximately between 2851ECh (+2,642,412d) and D7AE14h (–2,642,412d)—see Figure 52.

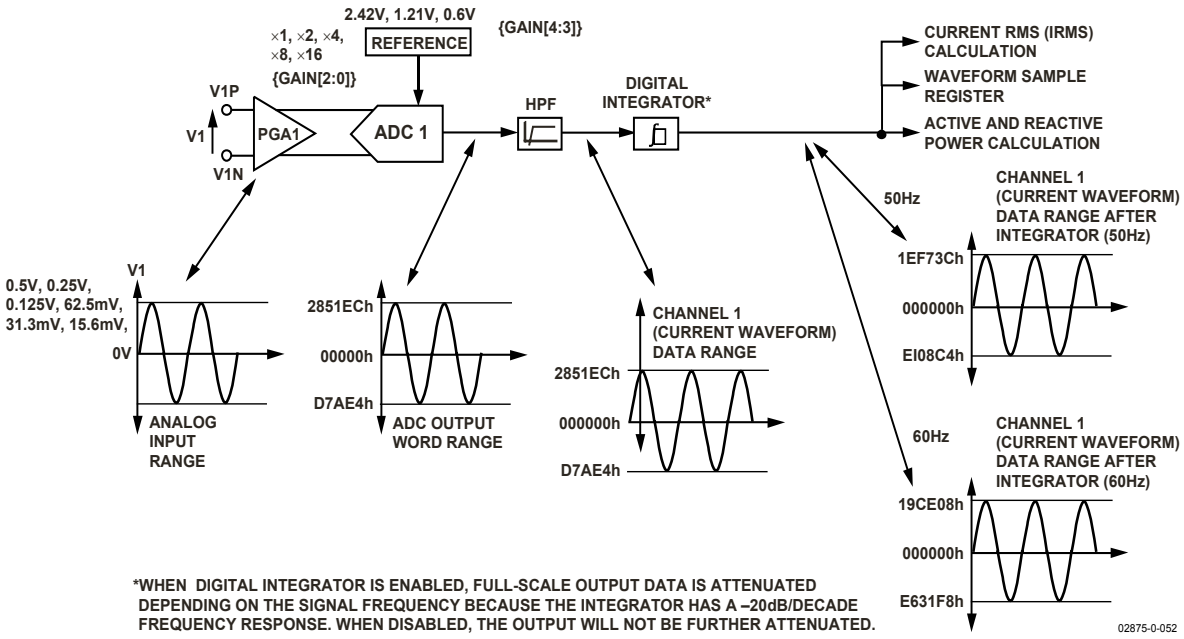

Figure 52. ADC and Signal Processing in Channel 1

Channel 1 Sampling

The waveform samples may also be routed to the waveform register (MODE[14:13] = 1,0) to be read by the system master (MCU). In waveform sampling mode, the WSMP bit (Bit 3) in the interrupt enable register must also be set to Logic 1. The active, apparent power, and energy calculation will remain uninterrupted during waveform sampling.

When in waveform sample mode, one of four output sample rates may be chosen by using Bits 11 and 12 of the mode register (WAVSEL1,0). The output sample rate may be 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see the Mode Register section. The interrupt request output, IRQ, signals a new sample availability by going active low. The timing is shown in Figure 53. The 24-bit waveform samples are transferred from the ADE7753 one byte (eight bits) at a time, with the most significant byte shifted out first. The 24-bit data-word is right justified—see the ADE7753 Serial Interface section. The interrupt request output IRQ stays low until the interrupt routine reads the reset status register—see the ADE7753 Interrupt section.

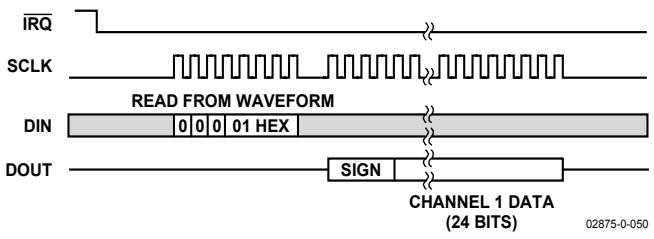

Figure 53. Waveform Sampling Channel 1

Channel 1 RMS Calculation

Root mean square (RMS) value of a continuous signal V(t) is defined as

$$V_{rms} = \sqrt{\frac{1}{T} \times \int_0^T V^2(t)dt} \quad (2)$$

For time sampling signals, RMS calculation involves squaring the signal, taking the average and obtaining the square root:

$$V_{rms} = \sqrt{\frac{1}{N} \times \sum_{i=1}^{N} V^2(i)} \quad (3)$$

ADE7753 calculates simultaneously the RMS values for Channel 1 and Channel 2 in different register. Figure 54 shows the detail of the signal processing chain for the RMS calculation on Channel 1. The Channel 1 RMS value is processed from the samples used in the Channel 1 waveform sampling mode. The Channel 1 RMS value is stored in an unsigned 24-bit register (IRMS). One LSB of the Channel 1 RMS register is equivalent to one LSB of a Channel 1 waveform sample. The update rate of the Channel 1 RMS measurement is CLKIN/4.

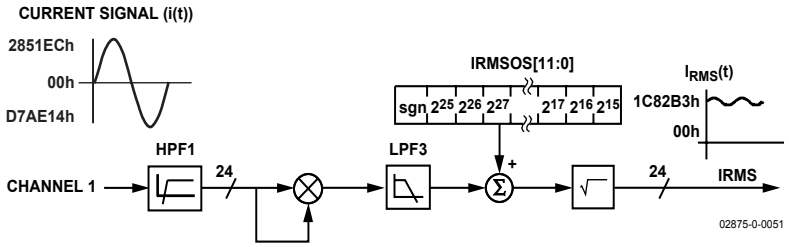

Figure 54. Channel 1 RMS Signal Processing

With the specified full-scale analog input signal of 0.5 V, the ADC will produce an output code that is approximately ±2,642,412d—see the Channel 1 ADC section. The equivalent RMS values of a full-scale ac signal are 1,868,467d (1C82B3h). The current RMS measurement provided in the ADE7753 is accurate to within 1% for signal input between full scale and full scale/100. The conversion from the register value to amps must be done externally in the microprocessor using an amps/LSB constant. To minimize noise, synchronize the reading of the rms register with the zero crossing of the voltage input and take the average of a number of readings.

Channel 1 RMS Offset Compensation

The ADE7753 incorporates a Channel 1 RMS offset compensation register (IRMSOS). This is a 12-bit signed register that can be used to remove offset in the Channel 1 RMS calculation. An offset may exist in the RMS calculation due to input noises that are integrated in the dc component of $V^2(t)$. The offset calibration will allow the content of the IRMS register to be maintained at 0 when no input is present on Channel 1.

One LSB of the Channel 1 RMS offset is equivalent to 32,768 LSB of the square of the Channel 1 RMS register. Assuming that the maximum value from the Channel 1 RMS calculation is 1,868,467d with full-scale ac inputs, then 1 LSB of the Channel 1 RMS offset represents 0.46% of measurement error at –60 dB down of full scale.

$$I_{rms} = \sqrt{{I_{rms_0}}^2 + IRMSOS \times 32768} \quad (4)$$

where I_{RMS0} is the RMS measurement without offset correction. To measure the offset of the RMS measurement, two data points are needed from non-zero input values, for example, the base current, Ib, and Imax/100. The offset can be calculated from these measurements.

CHANNEL 2 ADC

Channel 2 Sampling

In Channel 2 waveform sampling mode (MODE[14:13] = 1,1 and WSMP = 1), the ADC output code scaling for Channel 2 is not the same as Channel 1. The Channel 2 waveform sample is a 16-bit word and sign extended to 24 bits. For normal operation, the differential voltage signal between V2P and V2N should not exceed 0.5 V. With maximum voltage input (±0.5 V at PGA gain of 1), the output from the ADC swings between 2852h and D7AEh (±10,322d). However, before being passed to the waveform register, the ADC output is passed through a single-pole, low-pass filter with a cutoff frequency of 140 Hz. The plots in Figure 55 show the magnitude and phase response of this filter.

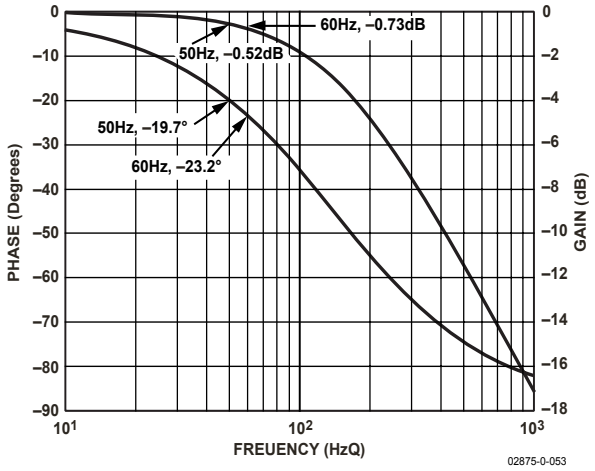

Figure 55. Magnitude and Phase Response of LPF1

The LPF1 has the effect of attenuating the signal. For example, if the line frequency is 60 Hz, then the signal at the output of LPF1 will be attenuated by about 8%.

$$\left|H(f)\right| = \frac{1}{\sqrt{1+\left(\frac{60\ Hz}{140\ Hz}\right)^2}} = 0.919 = -0.73\ dB \quad (5)$$

Note LPF1 does not affect the active power calculation. The signal processing chain in Channel 2 is illustrated in Figure 56.

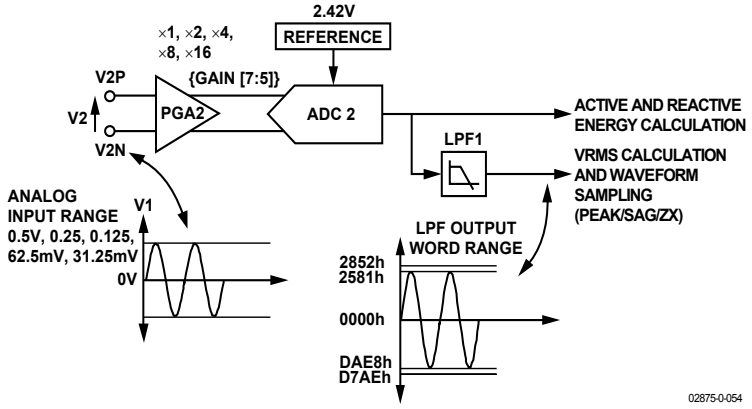

Figure 56. ADC and Signal Processing in Channel 2

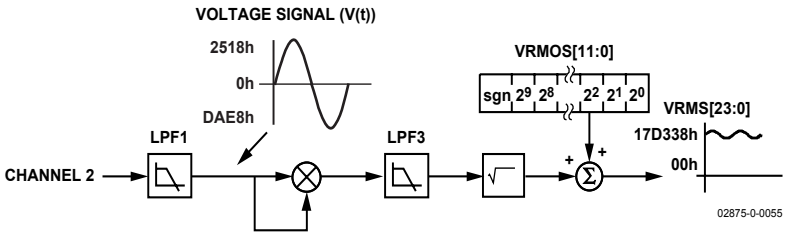

Figure 57. Channel 2 RMS Signal Processing

Channel 2 has only one analog input range (0.5 V differential). Like Channel 1, Channel 2 has a PGA with gain selections of 1, 2, 4, 8, and 16. For energy measurement, the output of the ADC is passed directly to the multiplier and is not filtered. An HPF is not required to remove any dc offset since it is only required to remove the offset from one channel to eliminate errors due to offsets in the power calculation. When in waveform sample mode, one of four output sample rates can be chosen by using Bits 11 and 12 of the mode register. The available output sample rates are 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see the Mode Register section. The interrupt request output IRQ signals that a sample is available by going active low. The timing is the same as that for Channel 1, as shown in Figure 53.

Channel 2 RMS Calculation

Figure 57 shows the details of the signal processing chain for the RMS calculation on Channel 2. The Channel 2 RMS value is processed from the samples used in the Channel 2 waveform sampling mode. The RMS value will be slightly attenuated because of LPF1. Channel 2 RMS value is stored in the unsigned 24-bit VRMS register. The update rate of the Channel 2 RMS measurement is CLKIN/4.

With the specified full-scale ac analog input signal of 0.5 V, the output from the LPF1 swings between 2518h and DAE8h at 60 Hz—see the Channel 2 ADC section. The equivalent RMS value of this full-scale ac signal is approximately 1,561,400 (17D338h) in the VRMS register. The voltage RMS measurement provided in the ADE7753 is accurate to within ±0.5% for signal input between full scale and full scale/20. The conversion from the register value to volts must be done externally in the microprocessor using a volts/LSB constant. Since the low-pass filtering used for calculating the RMS value is imperfect, there is some ripple noise from 2ω term present in the RMS measurement. To minimize the noise effect in the reading, synchronize the RMS reading with the zero crossings of the voltage input.

Channel 2 RMS Offset Compensation

The ADE7753 incorporates a Channel 2 RMS offset compensation register (VRMSOS). This is a 12-bit signed registers that can be used to remove offset in the Channel 2 RMS calculation. An offset may exist in the RMS calculation due to input noises and dc offset in the input samples. The offset calibration allows the contents of the VRMS register to be maintained at 0 when no voltage is applied. One LSB of the Channel 2 RMS offset is equivalent to one LSB of the RMS register. Assuming that the maximum value from the Channel 2 RMS calculation is 1,561,400d with full-scale ac inputs, then one LSB of the Channel 2 RMS offset represents 0.064% of measurement error at –60 dB down of full scale.

$$V_{rms} = V_{rmso} + VRMSOS \quad (6)$$

where V_{rmso} is the RMS measurement without offset correction. The voltage RMS offset compensation should be done by testing the RMS results at two non-zero input levels. One measurement can be done close to full scale and the other at approximately full scale/10. The voltage offset compensation can be derived from these measurements. If the voltage RMS offset register does not have enough range, the CH2OS register can also be used.

PHASE COMPENSATION

When the HPF is disabled, the phase error between Channel 1 and Channel 2 is 0 from dc to 3.5 kHz. When HPF is enabled, Channel 1 has a phase response illustrated in Figure 59 and Figure 60. Also shown in Figure 61 is the magnitude response of the filter. As can be seen from the plots, the phase response is almost 0 from 45 Hz to 1 kHz. This is all that is required in typical energy measurement applications. However, despite being internally phase compensated, the ADE7753 must work with transducers, which may have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a CT (current transformer). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7753 provides a means of digitally calibrating these small phase errors. The ADE7753 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for small phase errors. Because the compensation is in time, this technique should be used only for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique can introduce significant phase errors at higher harmonics.

The phase calibration register (PHCAL[5:0]) is a twos complement signed single-byte register that has values ranging from 21h (–31d) to 1Fh (31d).

The register is centered at 0Dh, so that writing 0Dh to the register gives 0 delay. By changing the PHCAL register, the time delay in the Channel 2 signal path can change from –102.12 µs to +39.96 µs (CLKIN = 3.579545 MHz). One LSB is equivalent to 2.22 µs (CLKIN/8) time delay or advance. A line frequency of 60 Hz gives a phase resolution of 0.048° at the fundamental (i.e., 360° × 2.22 µs × 60 Hz). Figure 58 illustrates how the phase compensation is used to remove a 0.1° phase lead in Channel 1 due to the external transducer. To cancel the lead (0.1°) in Channel 1, a phase lead must also be introduced into Channel 2. The resolution of the phase adjustment allows the introduction of a phase lead in increment of 0.048°. The phase lead is achieved by introducing a time advance into Channel 2. A time advance of 4.48 µs is made by writing –2 (0Bh) to the time delay block, thus reducing the amount of time delay by 4.48 µs, or equivalently, a phase lead of approximately 0.1° at line frequency of 60 Hz. 0Bh represents –2 because the register is centered with 0 at 0Dh.

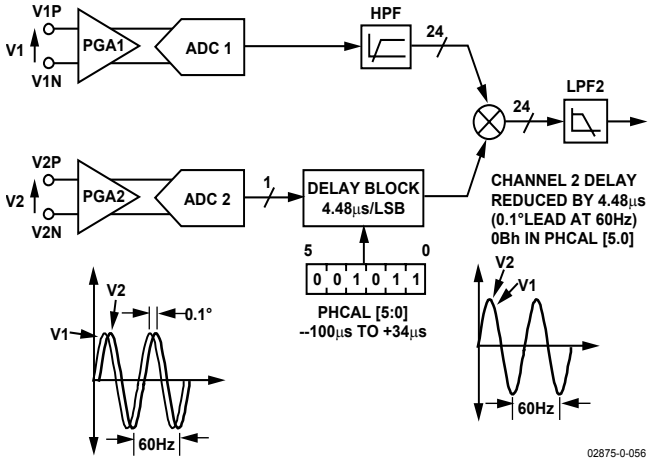

Figure 58. Phase Calibration

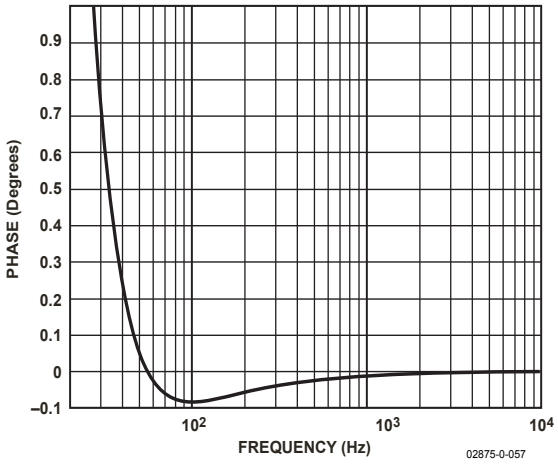

Figure 59. Combined Phase Response of the HPF and Phase Compensation (10 Hz to 1 kHz)

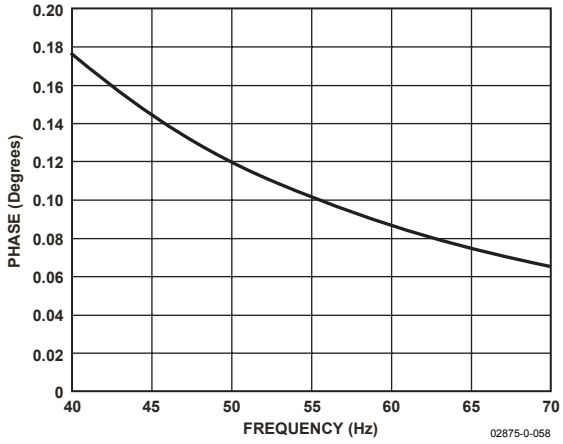

Figure 60. Combined Phase Response of the HPF and Phase Compensation (40 Hz to 70 Hz)

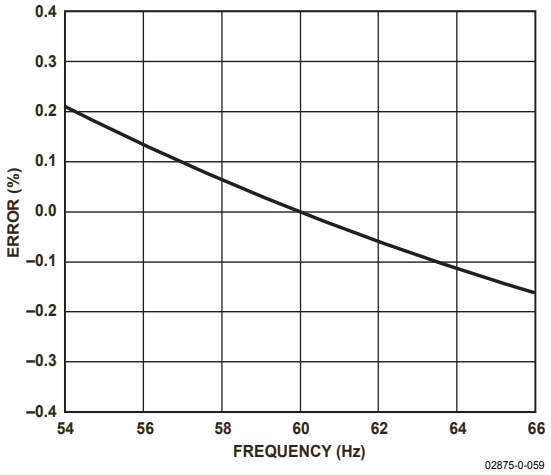

Figure 61. Combined Gain Response of the HPF and Phase Compensation

ACTIVE POWER CALCULATION

Power is defined as the rate of energy flow from source to load. It is defined as the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. Equation 9 gives an expression for the instantaneous power signal in an ac system.

$$v(t) = \sqrt{2} \times V \sin(\omega t) \quad (7)$$

$$i(t) = \sqrt{2} \times V \sin(\omega t) \quad (8)$$

where:

V is the RMS voltage.
I is the RMS current.

$$p(t) = v(t) \times i(t)$$

$$p(t) = VI - VI \cos(\omega t) \quad (9)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 10.

$$P = \frac{1}{nT} \int_0^{nT} p(t)dt = VI \quad (10)$$

where:

T is the line cycle period.
P is referred to as the active or real power.

Note that the active power is equal to the dc component of the instantaneous power signal *p(t)* in Equation 8, i.e., VI. This is the relationship used to calculate active power in the ADE7753.

The instantaneous power signal *p(t)* is generated by multiplying the current and voltage signals. The dc component of the instantaneous power signal is then extracted by LPF2 (low-pass filter) to obtain the active power information. This process is illustrated in Figure 62.

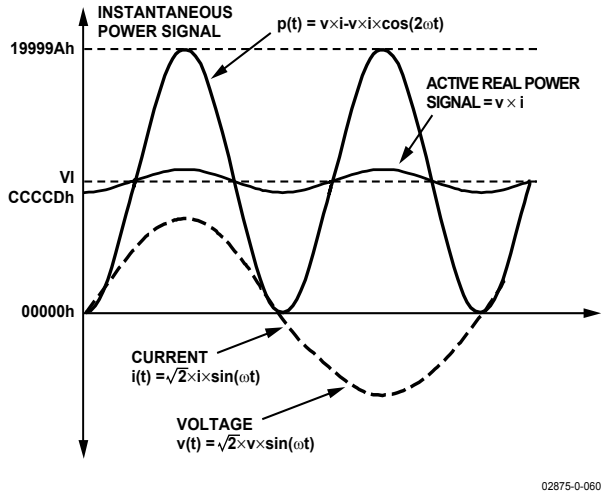

Figure 62. Active Power Calculation

Since LPF2 does not have an ideal "brick wall" frequency response—see Figure 63, the active power signal will have some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Since the ripple is sinusoidal in nature, it will be removed when the active power signal is integrated to calculate energy—see the Energy Calculation section.

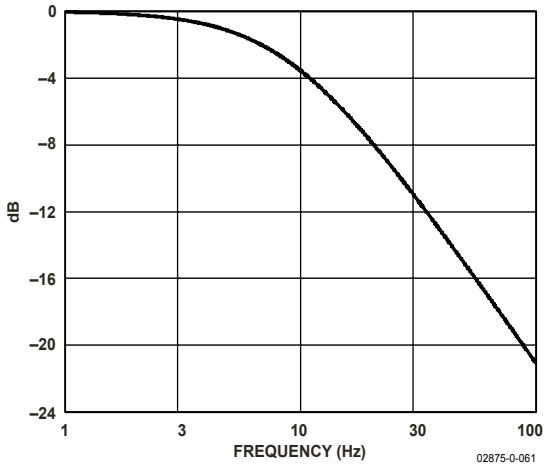

Figure 63. Frequency Response of LPF2

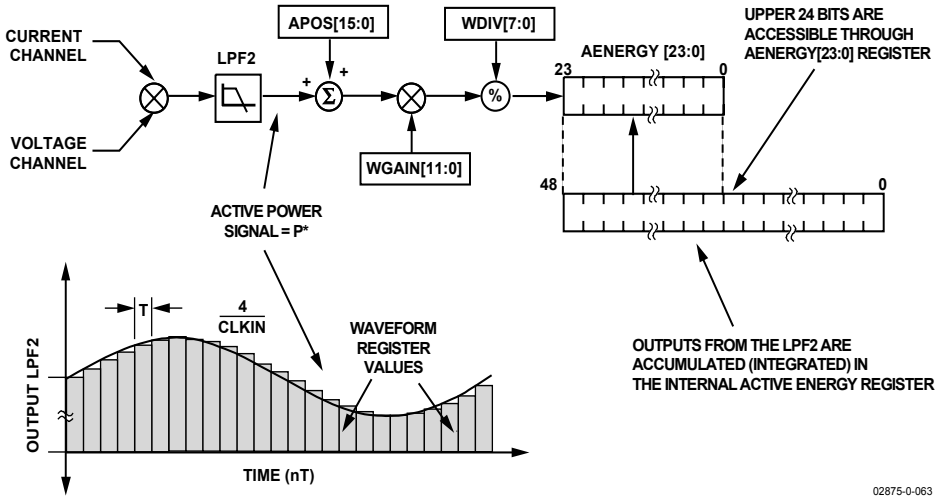

Figure 64. ADE7753 Active Energy Calculation

Figure 64 shows the signal processing chain for the active power calculation in the ADE7753. As explained, the active power is calculated by low-pass filtering the instantaneous power signal. Note that when reading the waveform samples from the output of LPF2, the gain of the active energy can be adjusted by using the multiplier and watt gain register (WGAIN[11:0]). The gain is adjusted by writing a twos complement 12-bit word to the watt gain register. Equation 11 shows how the gain adjustment is related to the contents of the watt gain register:

$$Output\ WGAIN = \left(Active\ Power \times \left\{ 1 + \frac{WGAIN}{2^{12}} \right\} \right) \qquad (11)$$

For example, when 7FFh is written to the watt gain register, the power output is scaled up by 50%. 7FFh = 2047d, $2047/2^{12} = 0.5$. Similarly, 800h = –2048d (signed twos complement) and power output is scaled by –50%. Each LSB scales the power output by 0.0244%. Figure 65 shows the maximum code (in hex) output range for the active power signal (LPF2). Note that the output range changes depending on the contents of the watt gain register. The minimum output range is given when the watt gain register contents are equal to 800h, and the maximum range is given by writing 7FFh to the watt gain register. This can be used to calibrate the active power (or energy) calculation in the ADE7753.

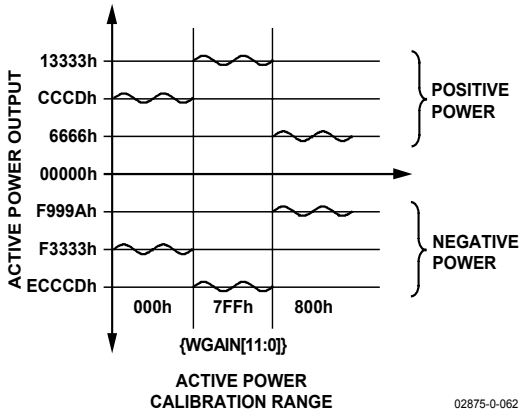

Figure 65. Active Power Calculation Output Range

Energy Calculation

As stated earlier, power is defined as the rate of energy flow. This relationship can be expressed mathematically in Equation 12.

$$P = \frac{dE}{dt} \qquad (12)$$

where:

P is power.
E is energy.

Conversely, energy is given as the integral of power.

$$E = \int P dt \qquad (13)$$

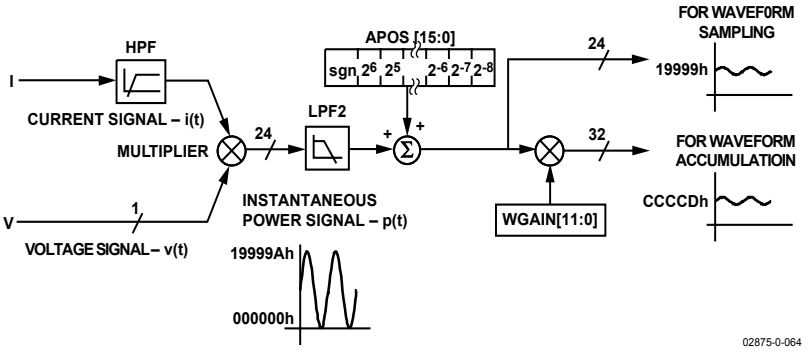

Figure 66. Active Power Signal Processing

The ADE7753 achieves the integration of the active power signal by continuously accumulating the active power signal in an internal non-readable 49-bit energy register. The active energy register (AENERGY[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 14 expresses the relationship.

$$E = \int p(t)dt = \underset{t \to 0}{Lim} \left\{ \sum_{n=1}^{\infty} p(nT) \times T \right\} \quad (14)$$

where:

n is the discrete time sample number.
T is the sample period.

The discrete time sample period (*T*) for the accumulation register in the ADE7753 is 1.1µs (4/CLKIN). As well as calculating the energy, this integration removes any sinusoidal components that may be in the active power signal. Figure 66 shows this discrete time integration or accumulation. The active power signal in the waveform register is continuously added to the internal active energy register. This addition is a signed addition; therefore negative energy will be subtracted from the active energy contents. The exception to this is when POAM is selected in the MODE[15:0] register. In this case, only positive energy contributes to the active energy accumulation—see the Positive-Only Accumulation Mode section.

The output of the multiplier is divided by WDIV. If the value in the WDIV register is equal to 0, then the internal active energy register is divided by 1. WDIV is an 8-bit unsigned register. After dividing by WDIV, the active energy is accumulated in a 49-bit internal energy accumulation register. The upper 24 bits of this register are accessible through a read to the active energy register (AENERGY[23:0]). A read to the RAENERGY register will return the content of the AENERGY register and the upper 24 bits of the internal register are cleared. As shown in Figure 66, the active power signal is accumulated in an internal 49-bit signed register. The active power signal can be read from the waveform register by setting MODE[14:13] = 0,0 and setting the WSMP bit (Bit 3) in the interrupt enable register to 1. Like the Channel 1 and Channel 2 waveform sampling modes, the waveform date is available at sample rates of 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see Figure 53.

Figure 67 shows this energy accumulation for full-scale signals (sinusoidal) on the analog inputs. The three curves displayed illustrate the minimum period of time it takes the energy register to roll over when the active power gain register contents are 7FFh, 000h, and 800h. The watt gain register is used to carry out power calibration in the ADE7753. As shown, the fastest integration time will occur when the watt gain register is set to maximum full scale, i.e., 7FFh.

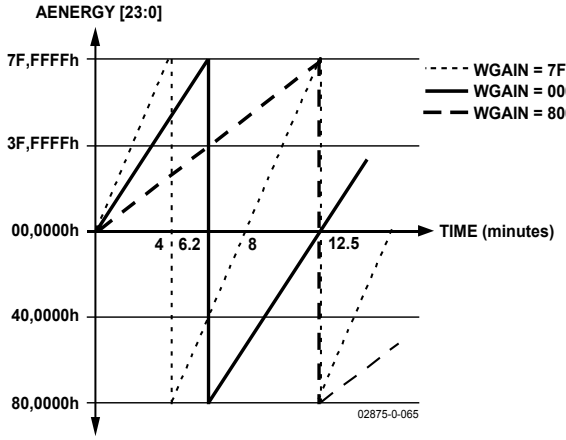

Figure 67. Energy Register Rollover Time for Full-Scale Power (Minimum and Maximum Power Gain)

Note that the energy register contents will roll over to full-scale negative (800000h) and continue increasing in value when the power or energy flow is positive—see Figure 67. Conversely, if the power is negative, the energy register would underflow to full-scale positive (7FFFFFh) and continue decreasing in value.

By using the interrupt enable register, the ADE7753 can be configured to issue an interrupt (IRQ) when the active energy register is half-full (positive or negative) or when an overflow or underflow occurs.

Integration Time under Steady Load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.1 µs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs and the WGAIN register set to 000h, the average word value from each LPF2 is CCCCDh—see Figure 62. The maximum positive value that can be stored in the internal 49-bit register is 2^{48} or FFFF,FFFF,FFFFh before it overflows. The integration time under these conditions with WDIV = 0 is calculated as follows:

$$Time = \frac{FFFF,FFFF,FFFFh}{CCCCDh} \times 1.12\mu s = 375.8s = 6.26\text{min} \quad (15)$$

When WDIV is set to a value different from 0, the integration time varies, as shown on Equation 16.

$$Time = Time_{WDIV=0} \times WDIV \quad (16)$$

Power Offset Calibration

The ADE7753 also incorporates an active power offset register (APOS[15:0]). This is a signed twos complement 16-bit register that can be used to remove offsets in the active power calculation—see Figure 66. An offset may exist in the power calculation due to crosstalk between channels on the PCB or in the IC itself. The offset calibration will allow the contents of the active power register to be maintained at 0 when no power is being consumed.

The 256 LSBs (APOS = 0100h) written to the active power offset register are equivalent to 1 LSB in the waveform sample register. Assuming the average value, output from LPF2 is CCCCDh (838,861d) when inputs on Channels 1 and 2 are both at full- cale. At −60 dB down on Channel 1 (1/1000 of the Channel 1 full-scale input), the average word value output from LPF2 is 838.861 (838,861/1,000). One LSB in the LPF2 output has a measurement error of 1/838.861 × 100% = 0.119% of the average value. The active power offset register has a resolution equal to 1/256 LSB of the waveform register, therefore the power offset correction resolution is 0.00047%/LSB (0.119%/256) at –60 dB.

ENERGY-TO-FREQUENCY CONVERSION

ADE7753 also provides energy-to-frequency conversion for calibration purposes. After initial calibration at manufacturing, the manufacturer or end customer will often verify the energy meter calibration. One convenient way to verify the meter calibration is for the manufacturer to provide an output frequency, which is proportional to the energy or active power under steady load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 68 illustrates the energy-to-frequency conversion in the ADE7753.

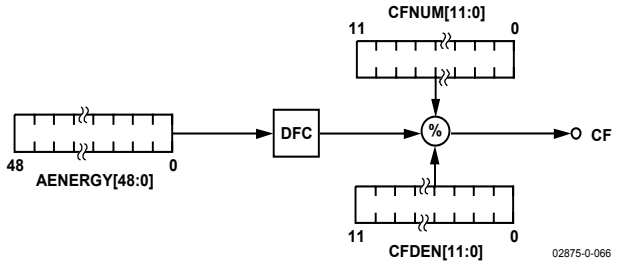

Figure 68. ADE7753 Energy-to-Frequency Conversion

A digital-to-frequency converter (DFC) is used to generate the CF pulsed output. The DFC generates a pulse each time 1 LSB in the active energy register is accumulated. An output pulse is generated when (CFDEN + 1)/(CFNUM + 1) number of pulses are generated at the DFC output. Under steady load conditions, the output frequency is proportional to the active power.

The maximum output frequency, with ac input signals at full scale and CFNUM = 00h and CFDEN = 00h, is approximately 23 kHz.

The ADE7753 incorporates two registers, CFNUM[11:0] and CFDEN[11:0], to set the CF frequency. These are unsigned 12-bit registers, which can be used to adjust the CF frequency to a wide range of values. These frequency-scaling registers are 12-bit registers, which can scale the output frequency by $1/2^{12}$ to 1 with a step of $1/2^{12}$.

If the value 0 is written to any of these registers, the value 1 would be applied to the register. The ratio (CFNUM + 1)/(CFDEN + 1) should be smaller than 1 to ensure proper operation. If the ratio of the registers (CFNUM + 1)/(CFDEN + 1) is greater than 1, the register values would be adjusted to a ratio (CFNUM + 1)/(CFDEN + 1) of 1. For example, if the output frequency is 1.562 kHz while the contents of CFDEN are 0 (000h), then the output frequency can be set to 6.1 Hz by writing FFh to the CFDEN register.

The output frequency will have a slight ripple at a frequency equal to twice the line frequency. This is due to imperfect filtering of the instantaneous power signal to generate the active power signal—see the Active Power Calculation section. Equation 8 gives an expression for the instantaneous power signal. This is filtered by LPF2 which has a magnitude response given by Equation 17.

$$|H(f)| = \frac{1}{\sqrt{1 + \frac{f^2}{8.9^2}}} \quad (17)$$

The active power signal (output of LPF2 can be rewritten as

$$p(t) = VI - \left[\frac{VI}{\sqrt{1+\left(\frac{2f_L}{8.9}\right)^2}} \right] \times \cos(4\pi f_L t) \quad (18)$$

where f_L is the line frequency, for example, 60 Hz.

From Equation 13,

$$E(t) = VIt - \left[\frac{VI}{4\pi f_L \sqrt{1+\left(\frac{2f_L}{8.9}\right)^2}} \right] \times \sin(4\pi f_L t) \quad (19)$$

From Equation 19 it can be seen that there is a small ripple in the energy calculation due to a sin(2ωt) component. This is shown graphically in Figure 69. The active energy calculation is shown by the dashed straight line and is equal to V × I × t. The sinusoidal ripple in the active energy calculation is also shown. Since the average value of a sinusoid is 0, this ripple will not contribute to the energy calculation over time. However, the ripple can be observed in the frequency output, especially at higher output frequencies. The ripple will get larger as a percentage of the frequency at larger loads and higher output frequencies. The reason is simply that at higher output frequencies the integration or averaging time in the energy-to-frequency conversion process is shorter. As a consequence, some of the sinusoidal ripple is observable in the frequency output. Choosing a lower output frequency at CF for calibration can significantly reduce the ripple. Also, averaging the output frequency by using a longer gate time for the counter will achieve the same results.

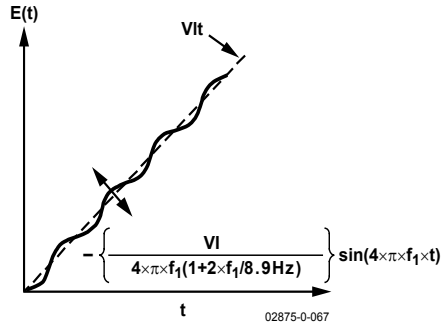

Figure 69. Output Frequency Ripple

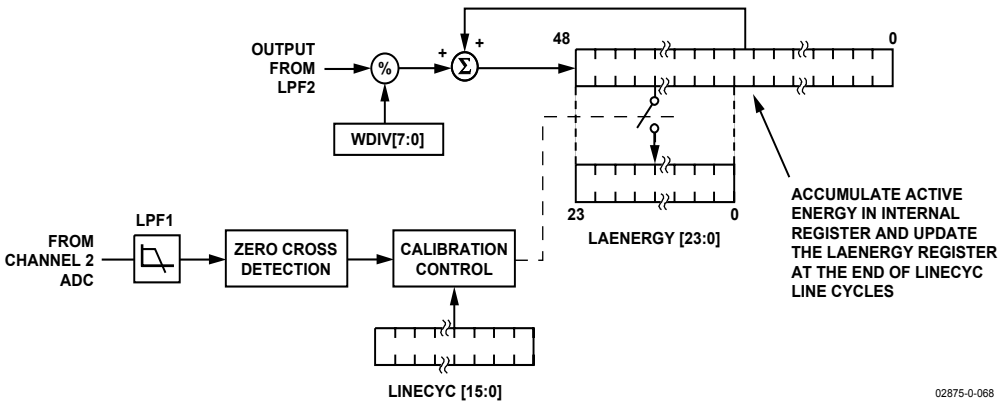

Figure 70. Energy Calculation Line Cycle Energy Accumulation Mode

LINE CYCLE ENERGY ACCUMULATION MODE

In line cycle energy accumulation mode, the energy accumulation of the ADE7753 can be synchronized to the Channel 2 zero crossing so that active energy can be accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of half line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation. Energy is calculated more accurately and in a shorter time because integration period can be shortened. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. The ADE7753 is placed in line cycle energy accumulation mode by setting Bit 7 (CYCMODE) in the mode register. In line cycle energy accumulation mode, the ADE7753 accumulates the active power signal in the LAENERGY register (Address 04h) for an integral number of line cycles, as shown in Figure 70. The number of half line cycles is specified in the LINECYC register (Address 1Ch). The ADE7753 can accumulate active power for up to 65,535 half line cycles. Because the active power is integrated on an integral number of line cycles, at the end of a line cycle energy accumulation cycle the CYCEND flag in the interrupt status register is set (Bit 2). If the CYCEND enable bit in the interrupt enable register is enabled, the IRQ output will also go active low. Thus the IRQ line can also be used to signal the completion of the line cycle energy accumulation. Another calibration cycle will start as long as the CYCMODE bit in the mode register is set.

From Equations 13 and 18,

$$E(t) = \int_0^{nT} VI\,dt - \left\{ \frac{VI}{\sqrt{1+\left(\frac{f}{8.9}\right)^2}} \right\} \times \int_0^{nT} \cos(2\pi f t)dt \qquad (20)$$

where:

n is a integer.
T is the line cycle period.

Since the sinusoidal component is integrated over a integer number of line cycles, its value is always 0. Therefore,

$$E = \int_0^{nT} VIdt + 0 \qquad (21)$$

$$E(t) = VInT \qquad (22)$$

Note that in this mode, the 16-bit LINECYC register can hold a maximum value of 65,535. In other words, the line energy accumulation mode can be used to accumulate active energy for a maximum duration over 65,535 half line cycles. At 60 Hz line frequency, it translates to a total duration of 65,535/120 Hz = 546 seconds.

POSITIVE-ONLY ACCUMULATION MODE

In positive-only accumulation mode, the energy accumulation is done only for positive power, ignoring any occurrence of negative power above or below the no load threshold, as shown in Figure 71. The CF pulse will also reflect this accumulation method when in this mode. The ADE7753 is placed in positive-only accumulation mode by setting the MSB of the mode register (MODE[15]). The default setting for this mode is off. Transitions in the direction of power flow, going from negative to positive or positive to negative, set the $\overline{\text{IRQ}}$ pin to active low if the interrupt enable register is enabled. The interrupt status registers, PPOS and PNEG, show which transition has occurred—see the ADE7753 register descriptions in Table 10.

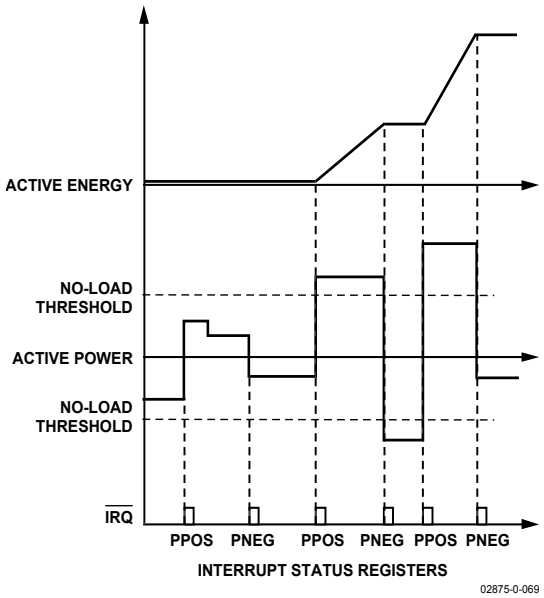

Figure 71. Energy Accumulation in Positive-Only Accumulation Mode

NO LOAD THRESHOLD

The ADE7753 includes a no-load threshold feature on the active energy that will eliminate any creep effects in the meter. The ADE7753 accomplishes this by not accumulating energy if the multiplier output is below the no load threshold. This threshold is 0.001% of the full-scale output frequency of the multiplier. Compare this value to the IEC1036 specification, which states that the meter must start up with a load equal to or less than 0.4% Ib. This standard translates to .0167% of the full-scale output frequency of the multiplier.

REACTIVE POWER CALCULATION

Reactive power is defined as the product of the voltage and current waveforms when one of these signals is phase-shifted by 90°. The resulting waveform is called the instantaneous reactive power signal. Equation 25 gives an expression for the instantaneous reactive power signal in an ac system when the phase of the current channel is shifted by +90°.

$$v(t) = \sqrt{2}\,V \sin(\omega t + \theta) \quad (23)$$
$$i(t)\sqrt{2}\,I \sin(\omega t)$$

$$i'(t) = \sqrt{2}\,I \sin(\omega t + \frac{\pi}{2}) \quad (24)$$

where:

θ is the phase difference between the voltage and current channel.
V is the RMS voltage.
I is the RMS current.

$$Rp(t) = v(t) \times i'(t)$$
$$Rp(t) = VI \sin(\theta) + VI \sin(2\omega t + \theta) \quad (25)$$

The average power over an integral number of lines (n) is given in Equation 26.

$$RP = \frac{1}{nT}\int_0^{nT} Rp(t)dt = VI \sin(\theta) \quad (26)$$

where:

T is the line cycle period.
RP is referred to as the reactive power.

Note that the reactive power is equal to the dc component of the instantaneous reactive power signal $Rp(t)$ in Equation 25. This is the relationship used to calculate reactive power in the ADE7753. The instantaneous reactive power signal $Rp(t)$ is generated by multiplying Channel 1 and Channel 2. In this case, the phase of Channel 1 is shifted by +90°. The dc component of the instantaneous reactive power signal is then extracted by a low-pass filter in order to obtain the reactive power information. Figure 72 shows the signal processing in the reactive power calculation in the ADE7753.

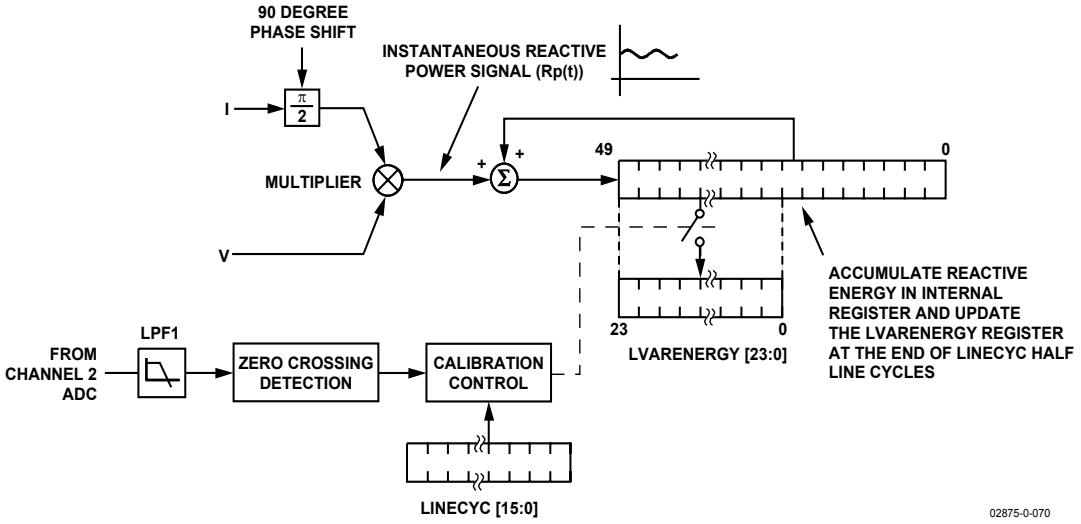

Figure 72. Reactive Power Signal Processing

The features of the line reactive energy accumulation are the same as the line active energy accumulation. The number of half line cycles is specified in the LINECYC register. LINECYC is an unsigned 16-bit register. The ADE7753 can accumulate reactive power for up to 65535 combined half cycles. At the end of an energy calibration cycle, the CYCEND flag in the interrupt status register is set. If the CYCEND mask bit in the interrupt mask register is enabled, the IRQ output will also go active low. Thus the IRQ line can also be used to signal the end of a calibration. The ADE7753 accumulates the reactive power signal in the LVARENERGY register for an integer number of half cycles, as shown in Figure 72.

SIGN OF REACTIVE POWER CALCULATION

Note that the average reactive power is a signed calculation. The phase shift filter has –90° phase shift when the integrator is enabled, and +90° phase shift when the integrator is disabled. Table 7 summarizes the relationship between the phase difference between the voltage and the current and the sign of the resulting VAR calculation.

Table 7. Sign of Reactive Power Calculation

Angle	Integrator	Sign
Between 0° to 90°	Off	Positive
Between –90° to 0°	Off	Negative
Between 0° to 90°	On	Positive
Between –90° to 0°	On	Negative

APPARENT POWER CALCULATION

The apparent power is defined as the maximum power that can be delivered to a load. V_{rms} and I_{rms} are the effective voltage and current delivered to the load; the apparent power (AP) is defined as $V_{rms} \times I_{rms}$. The angle θ between the active power and the apparent power generally represents the phase shift due to non-resistive loads. For single-phase applications, θ represents the angle between the voltage and the current signals—see Figure 73. Equation 28 gives an expression of the instantaneous power signal in an ac system with a phase shift.

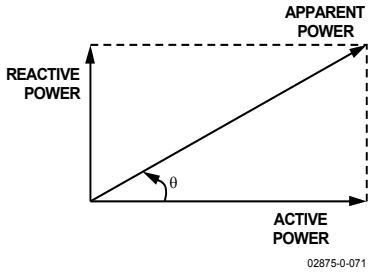

Figure 73. Power Triangle

$$v(t) = \sqrt{2}\, V_{rms} \sin(\omega t)$$

$$i(t) = \sqrt{2} I_{rms} \sin(\omega t + \theta) \quad (27)$$

$$p(t) = v(t) \times i(t)$$

$$p(t) = V_{rms}\ I_{rms} \cos(\theta) - V_{rms}\ I_{rms} \cos(2\omega t + \theta) \quad (28)$$

The apparent power is defined as $V_{rms} \times I_{rms}$. This expression is independent from the phase angle between the current and the voltage.

Figure 74 illustrates the signal processing in each phase for the calculation of the apparent power in the ADE7753.

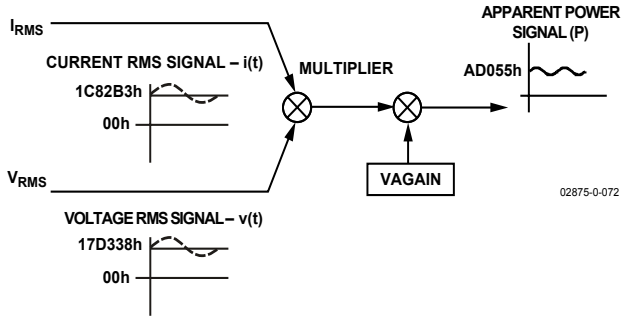

Figure 74. Apparent Power Signal Processing

The gain of the apparent energy can be adjusted by using the multiplier and VA gain register (VAGAIN[11:0]). The gain is adjusted by writing a twos complement, 12-bit word to the VA gain register. Equation 29 shows how the gain adjustment is related to the contents of the VA gain register.

$$OutputVAGAIN = \left(Apparent\ Power \times \left\{ 1 + \frac{VAGAIN}{2^{12}} \right\} \right) \quad (29)$$

For example, when 7FFh is written to the VA gain register, the power output is scaled up by 50%. 7FFh = 2047d, $2047/2^{12} = 0.5$. Similarly, 800h = –2047d (signed twos complement) and power output is scaled by –50%. Each LSB represents 0.0244% of the power output. The apparent power is calculated with the current and voltage RMS values obtained in the RMS blocks of the ADE7753. Figure 75 shows the maximum code (hexadecimal) output range of the apparent power signal. Note that the output range changes depending on the contents of the apparent power gain registers. The minimum output range is given when the apparent power gain register content is equal to 800h and the maximum range is given by writing 7FFh to the apparent power gain register. This can be used to calibrate the apparent power (or energy) calculation in the ADE7753.

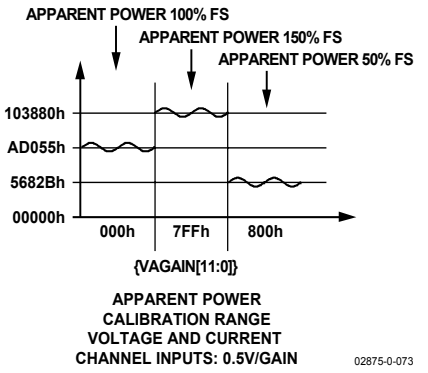

Figure 75. Apparent Power Calculation Output Range

Apparent Power Offset Calibration

Each RMS measurement includes an offset compensation register to calibrate and eliminate the dc component in the RMS value—see Channel 1 RMS calculation and Channel 2 RMS calculation sections. The Channel 1 and Channel 2 RMS values are then multiplied together in the apparent power signal processing. Since no additional offsets are created in the multiplication of the RMS values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement is done by calibrating each individual RMS measurement.

APPARENT ENERGY CALCULATION

The apparent energy is given as the integral of the apparent power.

$$Apparent\ Energy = \int Apparent\ Power(t)\ dt \qquad (30)$$

The ADE7753 achieves the integration of the apparent power signal by continuously accumulating the apparent power signal in an internal 48-bit register. The apparent energy register (VAENERGY[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 33 expresses the relationship

$$Apparent\ Energy = \underset{T\to 0}{Lim}\left\{\sum_{n=0}^{\infty} Apparent\ Power(nT)\times T\right\} \qquad (31)$$

where:

n is the discrete time sample number.
T is the sample period.

The discrete time sample period (T) for the accumulation register in the ADE7753 is 1.1 µs (4/CLKIN).

Figure 76 shows this discrete time integration or accumulation. The apparent power signal is continuously added to the internal register. This addition is a signed addition even if the apparent energy remains theoretically always positive.

The 49 bits of the internal register are divided by VADIV. If the value in the VADIV register is 0, then the internal active energy register is divided by 1. VADIV is an 8-bit unsigned register. The upper 24 bits are then written in the 24-bit apparent energy register (VAENERGY[23:0]). RVAENERGY register (24 bits long) is provided to read the apparent energy. This register is reset to 0 after a read operation.

Figure 77 shows this apparent energy accumulation for full-scale signals (sinusoidal) on the analog inputs. The three curves displayed illustrate the minimum time it takes the energy register to roll over when the VA gain registers content is equal to 7FFh, 000h, and 800h. The VA gain register is used to carry out an apparent power calibration in the ADE7753. As shown, the fastest integration time will occur when the VA gain register is set to maximum full scale, i.e., 7FFh.

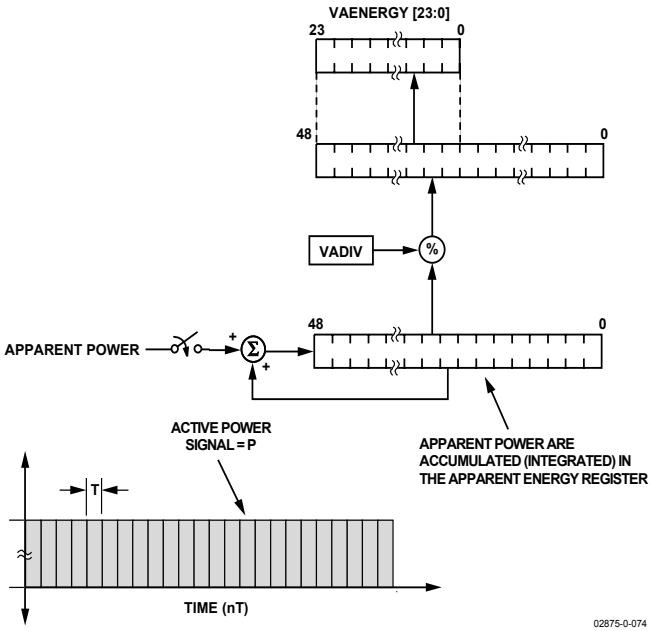

Figure 76. ADE7753 Apparent Energy Calculation

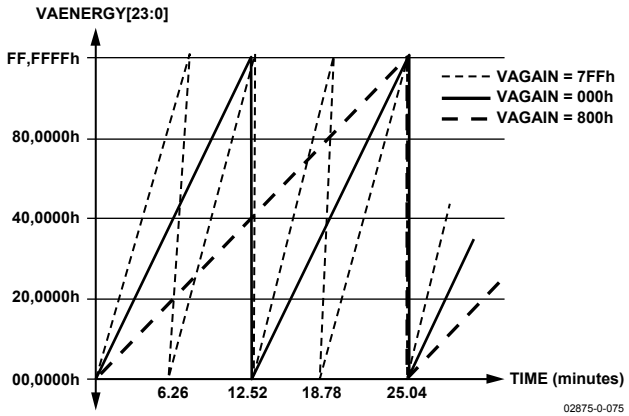

Figure 77. Energy Register Rollover Time for Full-Scale Power (Maximum and Minimum Power Gain)

Note that the apparent energy register contents roll over to full-scale negative (80,0000h) and continue increasing in value when the power or energy flow is positive—see Figure 77. By using the interrupt enable register, the ADE7753 can be configured to issue an interrupt (IRQ) when the apparent energy register is half full (positive or negative) or when an overflow/underflow occurs.

Integration Times under Steady Load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.1 µs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs and the VAGAIN register set to 000h, the average word value from apparent power stage is AD055h—see the Apparent Power Output Range section. The maximum value that can be stored in the apparent energy register before it overflows is 2^{24} or FF,FFFFh. The average word value is added to the internal register, which can store 2^{48} or FFFF,FFFF,FFFFh before it overflows. Therefore, the integration time under these conditions with VADIV = 0 is calculated as follows:

$$Time = \frac{FFFFFFFFFFFF}{AD055h} \times 1.2\mu s = 888s = 12.52\min \quad (32)$$

When VADIV is set to a value different from 0, the integration time varies, as shown on Equation 33.

$$Time = Time_{WDIV=0} \times VADIV \quad (33)$$

LINE APPARENT ENERGY ACCUMULATION

The ADE7753 is designed with a special apparent energy accumulation mode, which simplifies the calibration process. By using the on-chip zero-crossing detection, the ADE7753 accumulates the apparent power signal in the LVAENERGY register for an integral number of half cycles, as shown in Figure 78. The line apparent energy accumulation mode is always active.

The number of half line cycles is specified in the LINCYC register, which is an unsigned 16-bit register. The ADE7753 can accumulate apparent power for up to 65535 combined half cycles. Because the apparent power is integrated on the same integral number of line cycles as the line active energy register, these two values can be compared easily. The active energy and the apparent energy are calculated more accurately because of this precise timing control and provide all the information needed for reactive power and power factor calculation. At the end of an energy calibration cycle, the CYCEND flag in the interrupt status register is set. If the CYCEND mask bit in the interrupt mask register is enabled, the IRQ output will also go active low. Thus the IRQ line can also be used to signal the end of a calibration.

The line apparent energy accumulation uses the same signal path as the apparent energy accumulation. The LSB size of these two registers is equivalent.

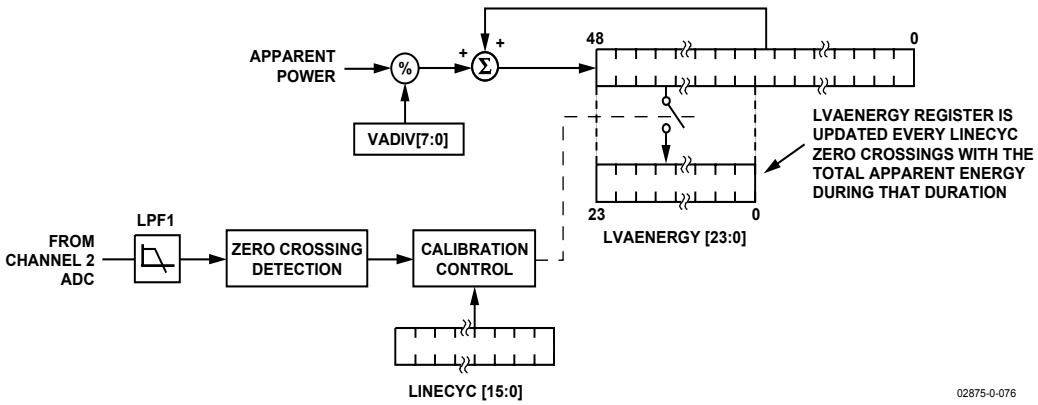

Figure 78. ADE7753 Apparent Energy Calibration

ENERGIES SCALING

The ADE7753 provides measurements of active, reactive, and apparent energies. These measurements do not have the same scaling and thus cannot be compared directly to each other.

Table 8. Energies Scaling

	PF = 1	PF = 0.707	PF = 0
Integrator On at 50 Hz			
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.983	Wh × 0.719
Apparent	Wh × 0.848	Wh × 0.848	Wh × 0.848
Integrator Off at 50 Hz			
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.491	Wh × 0.347
Apparent	Wh × 0.848	Wh × 0.848	Wh × 0.848
Integrator On at 60 Hz			
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.	Wh × 0.863
Apparent	Wh × 0.827	Wh × 0.827	Wh × 0.827
Integrator Off at 60 Hz			
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.409	Wh × 0.289
Apparent	Wh × 0.827	Wh × 0.827	Wh × 0.827

CALIBRATING THE ENERGY METER

When calibrating the ADE7753, the first step is to calibrate the frequency on CF to some required meter constant, e.g., 3200 imp/kWh.

A convenient way to determine the output frequency on CF is to use the line cycle energy accumulation mode. As shown in Figure 68, the DFC generates a pulse each time a LSB in the LAENERGY register is accumulated. CF frequency (before the CF frequency divider) can be conveniently determined by the following expression:

$$CF\ Frequency = \frac{Content\ of\ LAENERGY[23:0]\ Register}{Elapased\ Time} \quad (34)$$

When the CYCMODE bit (Bit 7) in the mode register is set to Logic 1, energy is accumulated over an integer number of half line cycles. If the line frequency is fixed and the number of half cycles of integration is specified, the total elapsed time can be calculated by the following:

$$Elapsed\ Time = \frac{1}{2 \times f_L} \times number\ of\ half\ cycles \quad (35)$$

For example, at 60 Hz line frequency, the elapsed time for 255 half cycles will be 2.125 seconds. Rewriting the above in terms of contents of various ADE7753 registers and line frequencies (f_L):

$$CF\ Frequency = \frac{LAENERGY[23:0] \times 2 \times f_L}{LINCYC[15:0]} \quad (36)$$

where f_L is the line frequency.

Alternatively, CF frequency can be calculated based on the average LPF2 output.

$$CF\ Frequency = \frac{Average\ LPF\ 2\ Output \times CLKIN}{2^{27}}$$

Calibrating the Frequency at CF

When the frequency before frequency division is known, the pair of CF frequency divider registers (CFNUM and CFDEN) can be adjusted to produce the required frequency on CF. In this example, a meter constant of 3200 imp/kWh is chosen as an appropriate constant. This means that under a steady load of 1 kW, the output frequency on CF would be

$$Frequency\ (CF) = \frac{3200\ imp/kWh}{60\ \text{min} \times 60\ \text{sec}} = \frac{3200}{3600} = 0.8888\ Hz \quad (37)$$

Assuming the meter is set up with a test current (basic current) of 20 A and a line voltage of 220 V for calibration, the load is calculated as 220 V × 20 A = 4.4 kW. Therefore the expected output frequency on CF under this steady load condition would be 4.4 × 0.8888 Hz = 3.9111 Hz. Under these load conditions, the transducers on Channel 1 and Channel 2 should be selected such that the signal on the voltage channel should see approximately half scale and the signal on the current channel about 1/8 of full scale (assuming a maximum current of 80 A). Assuming at line frequency of 60 Hz, energy is accumulated over FFh number of half line cycles; the resulting content of the LAENERGY register will be approximately 2971.4d). CF frequency is therefore calculated to be

$$Frequency\ (CF) = \frac{2971.4 \times 2 \times 60}{255} = 1398.3\ Hz \quad (38)$$

Alternatively, the average value from LPF2 under this condition is approximately 1/16 of the full-scale level. As described previously, the average LPF2 output at full-scale ac input is CCCCDh or 838,861d. At 1/16 of full scale, the LPF2 output is then 52,428.81. Then using digital-to-frequency conversion, the frequency under this load is calculated as

$$Frequency\ (CF) = \frac{52428.81 \times 3.579545\ MHz}{2^{27}} = 1398.3\ Hz \quad (39)$$

This is the frequency with the contents of the CFNUM and CFDEN registers equal to 000h. The desired frequency out is 3.9111 Hz. Therefore, the CF frequency must be divided by 2797/3.9111 Hz or 357.5d. This is achieved by loading the pair of CF divider registers with the closest rational number. In this case, the closest rational number is found to be 1/358 (or 1h/166h). Therefore, 0h and 165h should be written to the CFNUM and CFDEN registers, respectively. Note that the CF frequency is multiplied by the contents of (CFNUM + 1)/(CFDEN + 1). With the CF divide registers contents equal to 1h/166h, the output frequency is given as 2797 Hz/358 = 3.905 Hz. This setting has an error of –0.1%.

The critical part of this approach is that the exact line frequency needs to be known. If this is not possible, the frequency can be measured by using the period register of the ADE7753.

Note that changing WGAIN[11:0] register will also affect the output frequency from CF. The WGAIN register has a gain adjustment of 0.0244%/LSB.

Determine the kWHr/LSB Calibration Coefficient

The active energy register (AENERGY) can be used to calculate energy. A full description of this register can be found in the Energy Calculation section. The AENERGY register gives the user both sign and magnitude information regarding energy consumption. On completion of the CF frequency output calibration, i.e., after adjusting the CF frequency divider and the watt gain (WGAIN) register, the second stage of the calibration is to determine the kWh/LSB coefficient for the AENERGY register. Equation 40 shows how LAENERGY can be used to calculate the calibration coefficient.

$$kWHr/LSB = \frac{Calibration\ Power\ (in\ kW)}{3600\ \text{sec}onds/Hr} \times \frac{LINECYC[15:0]}{LAENERGY[23:0] \times 2 \times f_L} \quad (40)$$

CLKIN FREQUENCY

In this data sheet, the characteristics of the ADE7753 are shown with CLKIN frequency equals 3.579545 MHz. However, the ADE7753 is designed to have the same accuracy at any CLKIN frequency within the specified range. If the CLKIN frequency is not 3.579545 MHz, various timing and filter characteristics will need to be redefined with the new CLKIN frequency. For example, the cutoff frequencies of all digital filters such as LPF1, LPF2, or HPF1, will shift in proportion to the change in CLKIN frequency according to the following equation:

$$New\ Frequency = Original\ Frequency \times \frac{CLKIN\ Frequency}{3.579545\ MHz} \quad (41)$$

The change of CLKIN frequency does not affect the timing characteristics of the serial interface because the data transfer is synchronized with serial clock signal (SCLK). But one needs to observe the read/write timing of the serial data transfer—see the ADE7753 timing characteristics in Table 2. Table 9 lists various timing changes that are affected by CLKIN frequency.

Table 9. Frequency Dependencies of the ADE7753 Parameters

Parameter		CLKIN Dependency
Nyquist Frequency for CH 1 and CH 2 ADCs		CLKIN/8
PHCAL Resolution (Seconds per LSB)		4/CLKIN
Active Energy Register Update Rate (Hz)		CLKIN/4
Waveform Sampling Rate (Number of Samples per Second)		
WAVSEL 1,0 =	0 0	CLKIN/128
	0 1	CLKIN/256
	1 0	CLKIN/512
	1 1	CLKIN/1024
Maximum ZXTOUT Period		524,288/CLKIN

SUSPENDING ADE7753 FUNCTIONALITY

The analog and the digital circuit can be suspended separately. The analog portion of the ADE7753 can be suspended by setting the ASUSPEND bit (Bit 4) of the mode register to logic high—see the Mode Register section. In suspend mode, all waveform samples from the ADCs will be set to 0s. The digital circuitry can be halted by stopping the CLKIN input and maintaining a logic high or low on CLKIN pin. The ADE7753 can be reactivated by restoring the CLKIN input and setting the ASUSPEND bit to logic low.

CHECKSUM REGISTER

The ADE7753 has a checksum register (CHECKSUM[5:0]) to ensure the data bits received in the last serial read operation are not corrupted. The 6-bit checksum register is reset before the first bit (MSB of the register to be read) is put on the DOUT pin. During a serial read operation, when each data bit becomes available on the rising edge of SCLK, the bit will be added to the checksum register. In the end of the serial read operation, the content of the checksum register will equal to the sum of all ones in the register previously read. Using the checksum register, the user can determine if an error has occurred during the last read operation. Note that a read to the checksum register will also generate a checksum of the checksum register itself.

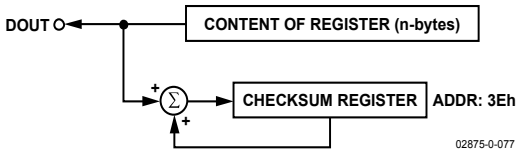

Figure 79. Checksum Register for Serial Interface Read

ADE7753 SERIAL INTERFACE

All ADE7753 functionality is accessible via several on-chip registers—see Figure 80. The contents of these registers can be updated or read using the on-chip serial interface. After power-on or toggling the $\overline{\text{RESET}}$ pin low or a falling edge on $\overline{\text{CS}}$, the ADE7753 is placed in communications mode. In communications mode, the ADE7753 expects a write to its communications register. The data written to the communications register determines whether the next data transfer operation will be a read or a write and also which register is accessed. Therefore all data transfer operations with the ADE7753, whether a read or a write, must begin with a write to the communications register.

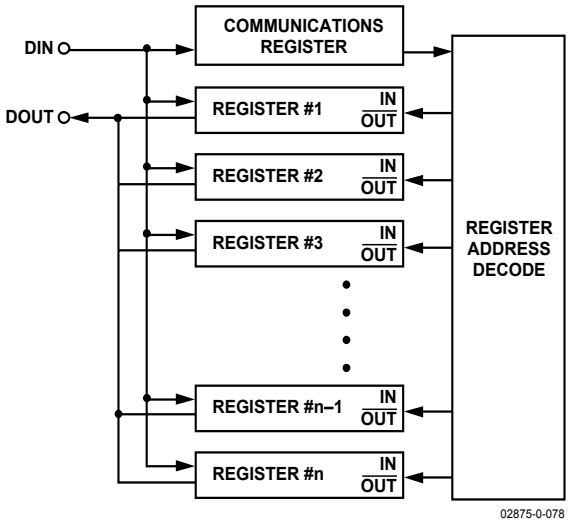

Figure 80. Addressing ADE7753 Registers via the Communications Register

The communications register is an 8-bit wide register. The MSB determines whether the next data transfer operation is a read or a write. The five LSBs contain the address of the register to be accessed—see the ADE7753 Communications Register section for a more detailed description.

Figure 81 and Figure 82 show the data transfer sequences for a read and write operation, respectively. On completion of a data transfer (read or write), the ADE7753 once again enters communications mode. A data transfer is complete when the LSB of the ADE7753 register being addressed (for a write or a read) is transferred to or from the ADE7753.

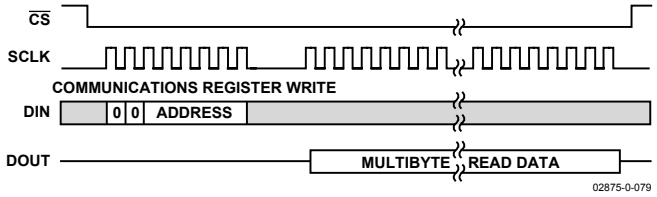

Figure 81. Reading Data from the ADE7753 via the Serial Interface

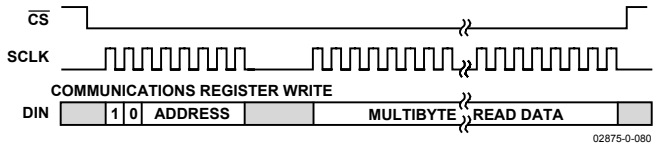

Figure 82. Writing Data to the ADE7753 via the Serial Interface

The serial interface of the ADE7753 is made up of four signals: SCLK, DIN, DOUT, and $\overline{\text{CS}}$. The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a Schmitt-trigger input structure that allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the ADE7753 at the DIN logic input on the falling edge of SCLK. Data is shifted out of the ADE7753 at the DOUT logic output on a rising edge of SCLK. The $\overline{\text{CS}}$ logic input is the chip-select input. This input is used when multiple devices share the serial bus. A falling edge on $\overline{\text{CS}}$ also resets the serial interface and places the ADE7753 into communications mode. The $\overline{\text{CS}}$ input should be driven low for the entire data transfer operation. Bringing $\overline{\text{CS}}$ high during a data transfer operation will abort the transfer and place the serial bus in a high impedance state. The $\overline{\text{CS}}$ logic input may be tied low if the ADE7753 is the only device on the serial bus. However, with $\overline{\text{CS}}$ tied low, all initiated data transfer operations must be fully completed, i.e., the LSB of each register must be transferred because there is no other way of bringing the ADE7753 back into communications mode without resetting the entire device, i.e., using $\overline{\text{RESET}}$.

ADE7753 Serial Write Operation

The serial write sequence takes place as follows. With the ADE7753 in communications mode (i.e., the $\overline{CS}$ input logic low), a write to the communications register first takes place. The MSB of this byte transfer is a 1, indicating that the data transfer operation is a write. The LSBs of this byte contain the address of the register to be written to. The ADE7753 starts shifting in the register data on the next falling edge of SCLK. All remaining bits of register data are shifted in on the falling edge of subsequent SCLK pulses—see Figure 82. As explained earlier, the data write is initiated by a write to the communications register followed by the data. During a data write operation to the ADE7753, data is transferred to all on-chip registers one byte at a time. After a byte is transferred into the serial port, there is a finite time before it is transferred to one of the ADE7753 on-chip registers. Although another byte transfer to the serial port can start while the previous byte is being transferred to an on-chip register, this second byte transfer should not finish until at least 4 μs after the end of the previous byte transfer. This functionality is expressed in the timing specification t_6—see Figure 82. If a write operation is aborted during a byte transfer ($\overline{CS}$ brought high), then that byte will not be written to the destination register.

Destination registers may be up to 3 bytes wide—see the ADE7753 Register Description tables. Therefore the first byte shifted into the serial port at DIN is transferred to the MSB (most significant byte) of the destination register. If, for example, the addressed register is 12 bits wide, a 2-byte data transfer must take place. The data is always assumed to be right justified, therefore in this case, the four MSBs of the first byte would be ignored and the four LSBs of the first byte written to the ADE7753 would be the four MSBs of the 12-bit word. Figure 84 illustrates this example.

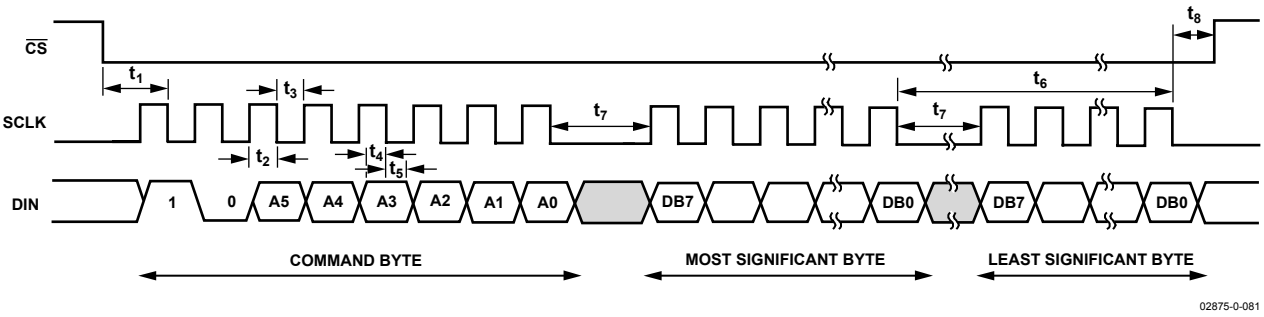

Figure 83. Serial Interface Write Timing

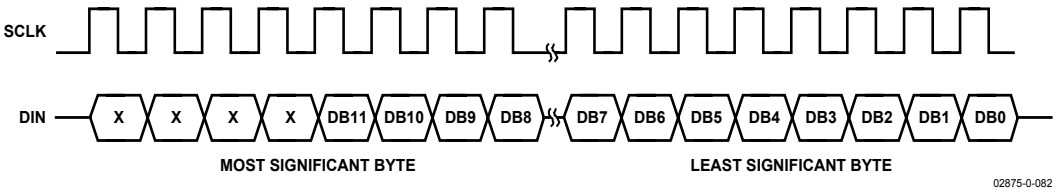

Figure 84. 12-Bit Serial Write Operation

ADE7753 Serial Read Operation

During a data read operation from the ADE7753, data is shifted out at the DOUT logic output on the rising edge of SCLK. As is the case with the data write operation, a data read must be preceded with a write to the communications register.

With the ADE7753 in communications mode (i.e., $\overline{CS}$ logic low), an 8-bit write to the communications register first takes place. The MSB of this byte transfer is a 0, indicating that the next data transfer operation is a read. The LSBs of this byte contain the address of the register that is to be read. The ADE7753 starts shifting out of the register data on the next rising edge of SCLK—see Figure 85. At this point, the DOUT logic output leaves its high impedance state and starts driving the data bus. All remaining bits of register data are shifted out on subsequent SCLK rising edges. The serial interface also enters communications mode again as soon as the read has been completed. At this point, the DOUT logic output enters a high impedance state on the falling edge of the last SCLK pulse. The read operation may be aborted by bringing the $\overline{CS}$ logic input high before the data transfer is complete. The DOUT output enters a high impedance state on the rising edge of $\overline{CS}$.

When an ADE7753 register is addressed for a read operation, the entire contents of that register are transferred to the serial port. This allows the ADE7753 to modify its on-chip registers without the risk of corrupting data during a multibyte transfer.

Note that when a read operation follows a write operation, the read command (i.e., write to communications register) should not happen for at least 4 μs after the end of the write operation. If the read command is sent within 4 μs of the write operation, the last byte of the write operation may be lost. This timing constraint is given as timing specification t_9.

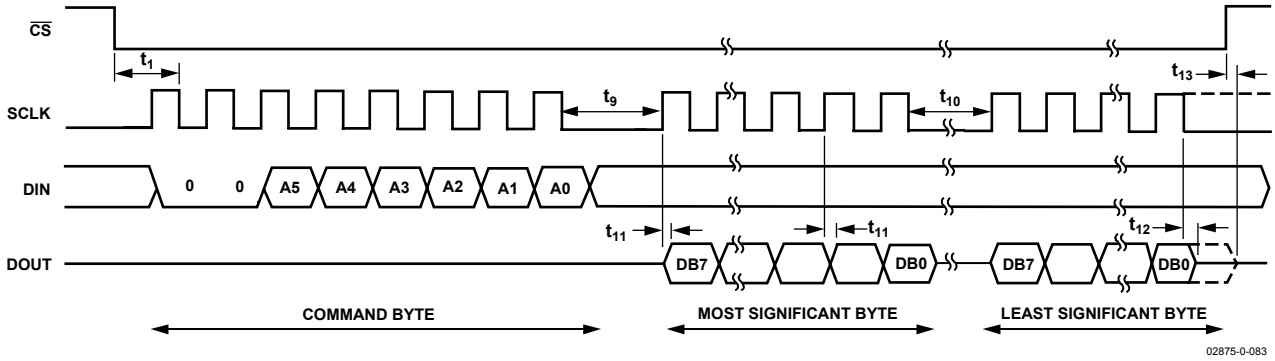

Figure 85. Serial Interface Read Timing

ADE7753 REGISTERS

Table 10. Summary of Registers by Address

Address	Name	R/W	No. Bits	Default	Description
01h	WAVEFORM	R	24	0h	Waveform Register. This read-only register contains the sampled waveform data from either Channel 1, Channel 2, or the active power signal. The data source and the length of the waveform registers are selected by data Bits 14 and 13 in the mode register—see the Channel 1 and Channel 2 Sampling section.
02h	AENERGY	R	24	0h	Active Energy Register. Active power is accumulated (integrated) over time in this 24-bit, read-only register—see the Energy Calculation section.
03h	RAENERGY	R	24	0h	Same as the active energy register except that the register is reset to 0 following a read operation.
04h	LAENERGY	R	24	0h	Line Accumulation Active Energy Register. The instantaneous active power is accumulated in this read-only register over the LINCYC number of half line cycles.
05h	VAENERGY	R	24	0h	Apparent Energy Register. Apparent power is accumulated over time in this read-only register.
06h	RVAENERGY	R	24	0h	Same as the VAENERGY register except that the register is reset to 0 following a read operation.
07h	LVAENERGY	R	24	0h	Line Accumulation Apparent Energy Register. The instantaneous real power is accumulated in this read-only register over the LINECYC number of half line cycles.
08h	LVARENERGY	R	24	0h	Line Accumulation Reactive Energy Register. The instantaneous reactive power is accumulated in this read-only register over the LINECYC number of half line cycles.
09h	MODE	R/W	16	000Ch	Mode Register. This is a 16-bit register through which most of the ADE7753 functionality is accessed. Signal sample rates, filter enabling, and calibration modes are selected by writing to this register. The contents may be read at any time—see the Mode Register section.
0Ah	IRQEN	R/W	16	40h	Interrupt Enable Register. ADE7753 interrupts may be deactivated at any time by setting the corresponding bit in this 16- bit enable register to Logic 0. The status register will continue to register an interrupt event even if disabled. However, the $\overline{\text{IRQ}}$ output will not be activated—see the ADE7753 Interrupts section.
0Bh	STATUS	R	16	0h	Interrupt Status Register. This is an 16-bit read-only register. The status register contains information regarding the source of ADE7753 interrupts—the see ADE7753 Interrupts section.
0Ch	RSTSTATUS	R	16	0h	Same as the interrupt status register except that the register contents are reset to 0 (all flags cleared) after a read operation.
0Dh	CH1OS	R/W	8	00h	Channel 1 Offset Adjust. Bit 6 is not used. Writing to Bits 0 to 5 allows offsets on Channel 1 to be removed—see the Analog Inputs and CH1OS Register sections. Writing a Logic 1 to the MSB of this register enables the digital integrator on Channel 1, a 0 disables the integrator. The default value of this bit is 0.
0Eh	CH2OS	R/W	8	0h	Channel 2 Offset Adjust. Bits 6 and 7 not used. Writing to Bits 0 to 5 of this register allows any offsets on Channel 2 to be removed—see the Analog Inputs section.
0Fh	GAIN	R/W	8	0h	PGA Gain Adjust. This 8-bit register is used to adjust the gain selection for the PGA in Channels 1 and 2—see the Analog Inputs section.
10h	PHCAL	R/W	6	0Dh	Phase Calibration Register. The phase relationship between Channel 1 and 2 can be adjusted by writing to this 6-bit register. The valid content of this twos compliment register is between 1Dh to 21h. At line frequency of 60 Hz, this is a range from –2.06° to +0.7°—see the Phase Compensation section.
11h	APOS	R/W	16	0h	Active Power Offset Correction. This 16-bit register allows small offsets in the active power calculation to be removed—see the Active Power Calculation section.
12h	WGAIN	R/W	12	0h	Power Gain Adjust. This is a 12-bit register. The active power calculation can be calibrated by writing to this register. The calibration range is ±50% of the nominal full-scale active power. The resolution of the gain adjust is 0.0244%/LSB —see the Channel 1 ADC Gain Adjust section.

Address	Name	R/W	No. Bits	Default	Description
13h	WDIV	R/W	8	0h	Active Energy Divider Register. The internal active energy register is divided by the value of this register before being stored in the AENERGY register.
14h	CFNUM	R/W	12	3Fh	CF Frequency Divider Numerator Register. The output frequency on the CF pin is adjusted by writing to this 12-bit read/write register—see the Energy-to-Frequency Conversion section.
15h	CFDEN	R/W	12	3Fh	CF Frequency Divider Denominator Register. The output frequency on the CF pin is adjusted by writing to this 12-bit read/write register—see the Energy-to-Frequency Conversion section.
16h	IRMS	R	24	0h	Channel 1 RMS Value (Current Channel).
17h	VRMS	R	24	0h	Channel 2 RMS Value (Voltage Channel).
18h	IRMSOS	R/W	12	0h	Channel 1 RMS Offset Correction Register.
19h	VRMSOS	R/W	12	0h	Channel 2 RMS Offset Correction Register.
1Ah	VAGAIN	R/W	12	0h	Apparent Gain Register. Apparent power calculation can be calibrated by writing this register. The calibration range is 50% of the nominal full-scale real power. The resolution of the gain adjust is 0.02444%/LSB.
1Bh	VADIV	R/W	8	0h	Apparent Energy Divider Register. The internal apparent energy register is divided by the value of this register before being stored in the VAENERGY register.
1Ch	LINECYC	R/W	16	FFFFh	Line Cycle Energy Accumulation Mode Line-Cycle Register. This 16-bit register is used during line cycle energy accumulation mode to set the number of half line cycles for energy accumulation—see the Line Cycle Energy Accumulation Mode section.
1Dh	ZXTOUT	R/W	12	FFFh	Zero-Cross Timeout. If no zero crossings are detected on Channel 2 within a time period specified by this 12-bit register, the interrupt request line ($\overline{IRQ}$) will be activated—see the Zero-Crossing Detection section.
1Eh	SAGCYC	R/W	8	FFh	Sag Line Cycle Register. This 8-bit register specifies the number of consecutive line cycles the signal on Channel 2 must be below SAGLVL before the SAG output is activated—see the Voltage Sag Detection section.
1Fh	SAGLVL	R/W	8	0h	Sag Voltage Level. An 8-bit write to this register determines at what peak signal level on Channel 2 the $\overline{SAG}$ pin will become active. The signal must remain low for the number of cycles specified in the SAGCYC register before the $\overline{SAG}$ pin is activated—see Line Voltage Sag Detection.
20h	IPKLVL	R/W	8	FFh	Channel 1 Peak Level Threshold (Current Channel). This register sets the level of the current peak detection. If the Channel 1 input exceeds this level, the PKI flag in the status register is set.
21h	VPKLVL	R/W	8	FFh	Channel 2 Peak Level Threshold (Voltage Channel). This register sets the level of the voltage peak detection. If the Channel 2 input exceeds this level, the PKV flag in the status register is set.
22h	IPEAK	R	24	0h	Channel 1 Peak Register. The maximum input value of the current channel since the last read of the register is stored in this register.
23h	RSTIPEAK	R	24	0h	Same as Channel 1 Peak Register except that the register contents are reset to 0 after read.
24h	VPEAK	R	24	0h	Channel 2 Peak Register. The maximum input value of the voltage channel since the last read of the register is stored in this register.
25h	RSTVPEAK	R	24	0h	Same as Channel 2 Peak Register except that the register contents are reset to 0 after a read.
26h	TEMP	R	8	0h	Temperature Register. This is an 8-bit register which contains the result of the latest temperature conversion—see the Temperature Measurement section.
27h	PERIOD	R	15	0h	Period of the Channel 2 (Voltage Channel) Input Estimated by Zero-Crossing Processing.
28h–3Ch					Reserved.
3Dh	TMODE	R/W	8	–	Test Mode Register.
3Eh	CHKSUM	R	6	0h	Checksum Register. This 6-bit read-only register is equal to the sum of all the ones in the previous read—see the ADE7753 Serial Read Operation section.
3Fh	DIEREV	R	8	–	Die Revision Register. This 8-bit read-only register contains the revision number of the silicon.

ADE7753 REGISTER DESCRIPTIONS

All ADE7753 functionality is accessed via the on-chip registers. Each register is accessed by first writing to the communications register and then transferring the register data. A full description of the serial interface protocol is given in the Serial Interface section.

COMMUNICATIONS REGISTER

The communications register is an 8-bit, write-only register which controls the serial data transfer between the ADE7753 and the host processor. All data transfer operations must begin with a write to the communications register. The data written to the communications register determines whether the next operation is a read or a write and which register is being accessed. Table 11 outlines the bit designations for the communications register.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W/R	0	A5	A4	A3	A2	A1	A0

Table 11. Communications Register

Bit Location	Bit Mnemonic	Description
0 to 5	A0 to A5	The six LSBs of the communications register specify the register for the data transfer operation. Table 10 lists the address of each ADE7753 on-chip register.
6	RESERVED	This bit is unused and should be set to 0.
7	W/R	When this bit is a Logic 1, the data transfer operation immediately following the write to the communications register will be interpreted as a write to the ADE7753. When this bit is a Logic 0, the data transfer operation immediately following the write to the communications register will be interpreted as a read operation.

MODE REGISTER (09H)

The ADE7753 functionality is configured by writing to the mode register. Table 12 summarizes the functionality of each bit in the mode register.

Table 12. Mode Register

Bit Location	Bit Mnemonic	Default Value	Description		
0	DISHPF	0	HPF (high-pass filter) in Channel 1 is disabled when this bit is set.		
1	DISLPF2	0	LPF (low-pass filter) after the multiplier (LPF2) is disabled when this bit is set.		
2	DISCF	1	Frequency output CF is disabled when this bit is set.		
3	DISSAG	1	Line voltage sag detection is disabled when this bit is set.		
4	ASUSPEND	0	By setting this bit to Logic 1, both ADE7753's A/D converters can be turned off. In normal operation, this bit should be left at Logic 0. All digital functionality can be stopped by suspending the clock signal at CLKIN pin.		
5	TEMPSEL	0	Temperature conversion starts when this bit is set to 1. This bit is automatically reset to 0 when the temperature conversion is finished.		
6	SWRST	0	Software Chip Reset. A data transfer should not take place to the ADE7753 for at least 18 µs after a software reset.		
7	CYCMODE	0	Setting this bit to Logic 1 places the chip into line cycle energy accumulation mode.		
8	DISCH1	0	ADC 1 (Channel 1) inputs are internally shorted together.		
9	DISCH2	0	ADC 2 (Channel 2) inputs are internally shorted together.		
10	SWAP	0	By setting this bit to Logic 1 the analog inputs V2P and V2N are connected to ADC 1 and the analog inputs V1P and V1N are connected to ADC 2.		
12, 11	DTRT1,0	00	These bits are used to select the waveform register update rate.		
			DTRT 1	DTRT0	Update Rate
			0	0	27.9 kSPS (CLKIN/128)
			0	1	14 kSPS (CLKIN/256)
			1	0	7 kSPS (CLKIN/512)
			1	1	3.5 kSPS (CLKIN/1024)

Bit Location	Bit Mnemonic	Default Value	Description
14, 13	WAVSEL1,0	00	These bits are used to select the source of the sampled data for the waveform register.

WAVSEL1,0	Length	Source
0	0	24 bits active power signal (output of LPF2)
0	1	Reserved
1	0	24 bits Channel 1
1	1	24 bits Channel 2

15	POAM	0	Writing Logic 1 to this bit will allow only positive power to be accumulated in the ADE7753. The default value of this bit is 0.

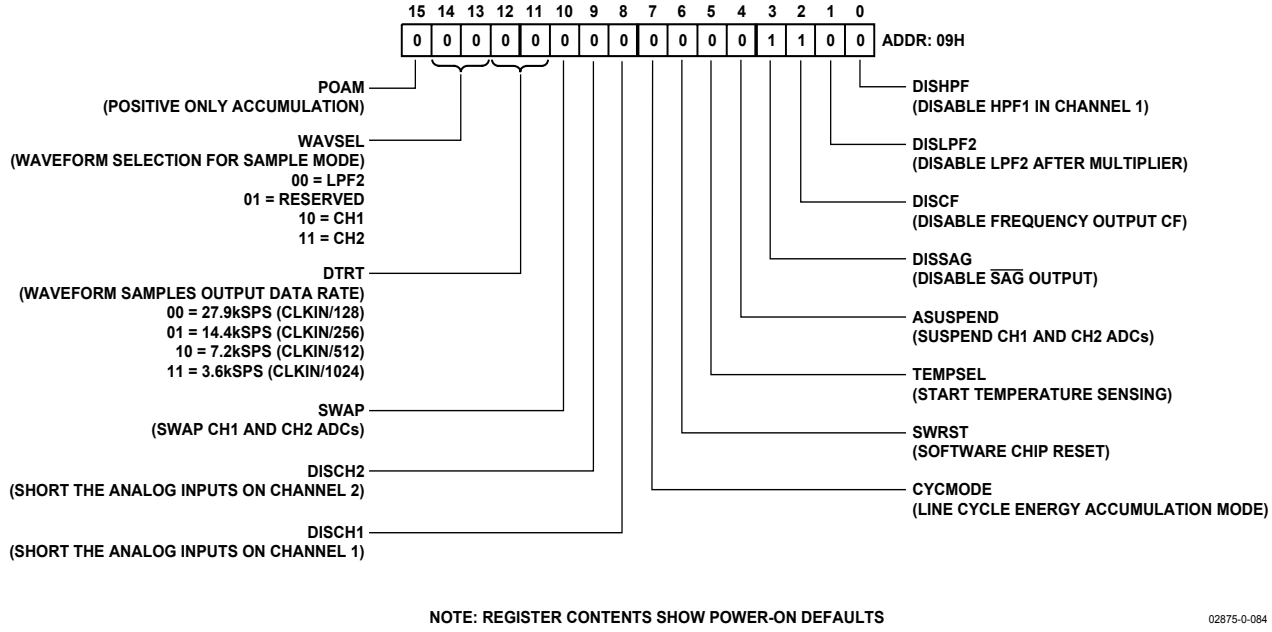

Figure 86. Mode Register

INTERRUPT STATUS REGISTER (0Bh), RESET INTERRUPT STATUS REGISTER (0Ch), INTERRUPT ENABLE REGISTER (0Ah)

The status register is used by the MCU to determine the source of an interrupt request (IRQ). When an interrupt event occurs in the ADE7753, the corresponding flag in the interrupt status register is set logic high. If the enable bit for this flag is Logic 1 in the interrupt enable register, the IRQ logic output goes active low. When the MCU services the interrupt, it must first carry out a read from the interrupt status register to determine the source of the interrupt.

Table 13. Interrupt Status Register, Reset Interrupt Status Register, and Interrupt Enable Register

Bit Location	Interrupt Flag	Description
0h	AEHF	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the active energy register (i.e., the AENERGY register is half full).
1h	SAG	Indicates that an interrupt was caused by a SAG on the line voltage.
2h	CYCEND	Indicates the end of energy accumulation over an integer number of half line cycles as defined by the content of the LINECYC register—see the Line Cycle Energy Accumulation Mode section.
3h	WSMP	Indicates that new data is present in the waveform register.
4h	ZX	This status bit reflects the status of the ZX logic ouput—see the Zero-Crosssing Detection section.

Bit Location	Interrupt Flag	Description
5h	TEMP	Indicates that a temperature conversion result is available in the temperature register.
6h	RESET	Indicates the end of a reset (for both software or hardware reset). The corresponding enable bit has no function in the interrupt enable register, i.e., this status bit is set at the end of a reset, but it cannot be enabled to cause an interrupt.
7h	AEOF	Indicates that the active energy register has overflowed.
8h	PKV	Indicates that waveform sample from Channel 2 has exceeded the VPKLVL value.
9h	PKI	Indicates that waveform sample from Channel 1 has exceeded the IPKLVL value.
Ah	VAEHF	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the apparent energy register, i.e., the VAENERGY register is half full.
Bh	VAEOF	Indicates that the apparent enrgy register has overflowed.
Ch	ZXTO	Indicates that an interrupt was caused by a missing zero crossing on the line voltage for the specified number of line cycles—see the Zero-Crosssing Timeout section.
Dh	PPOS	Indicates that the power has gone from negative to positive.
Eh	PNEG	Indicates that the power has gone from positive to negative.
Fh	RESERVED	Reserved.

CH1OS REGISTER (08h)

The CH1OS register is an 8-bit, read/write enabled register. The MSB of this register is used to switch on/off the digital integrator in Channel 1, and Bits 0 to 5 indicates the amount of the offset correction in Channel 1. Table 14 summarizes the function of this register.

Table 14. CH1OS Register

Bit Location	Bit Mnemonic	Description
0 to 5	OFFSET	The six LSBs of the CH1OS register control the amount of dc offset correction in Channel 1 ADC. The 6-bit offset correction is sign and magnitude coded. Bits 0 to 4 indicate the magnitude of the offset correction. Bit 5 shows the sign of the offset correction. A 0 in Bit 5 means the offset correction is positive and a 1 indicates the offset correction is negative.
6	Not Used	This bit is unused.
7	INTEGRATOR	This bit is used to activate the digital integrator on Channel 1. The digital integrator is switched on by setting this bit. This bit is set to be 0 on default.

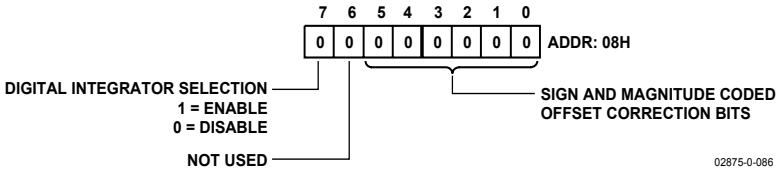

Figure 87. Channel 1 Offset Register

OUTLINE DIMENSIONS

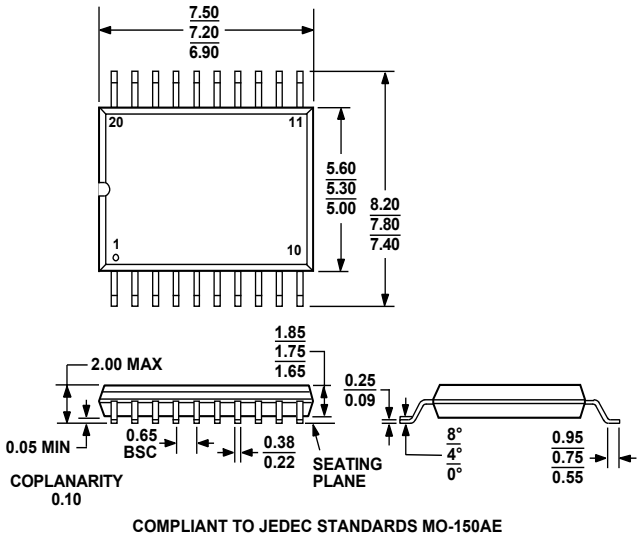

Figure 88. 20-Lead Shrink Small Outline Package [SSOP]

ORDERING GUIDE

Table 15.

Model	Package Description	Package Option*	Temperature Range
ADE7753ARS	20-Lead SSOP	RS-20	–40°C to +85°C
ADE7753ARSRL	20-Lead SSOP	RS-20	–40°C to +85°C
EVAL-ADE7753EB	ADE7753 Evaluation Board		–40°C to +85°C

NOTES

C02875-0-8/03(0)